NAVAL RESEARCH REVIEWS

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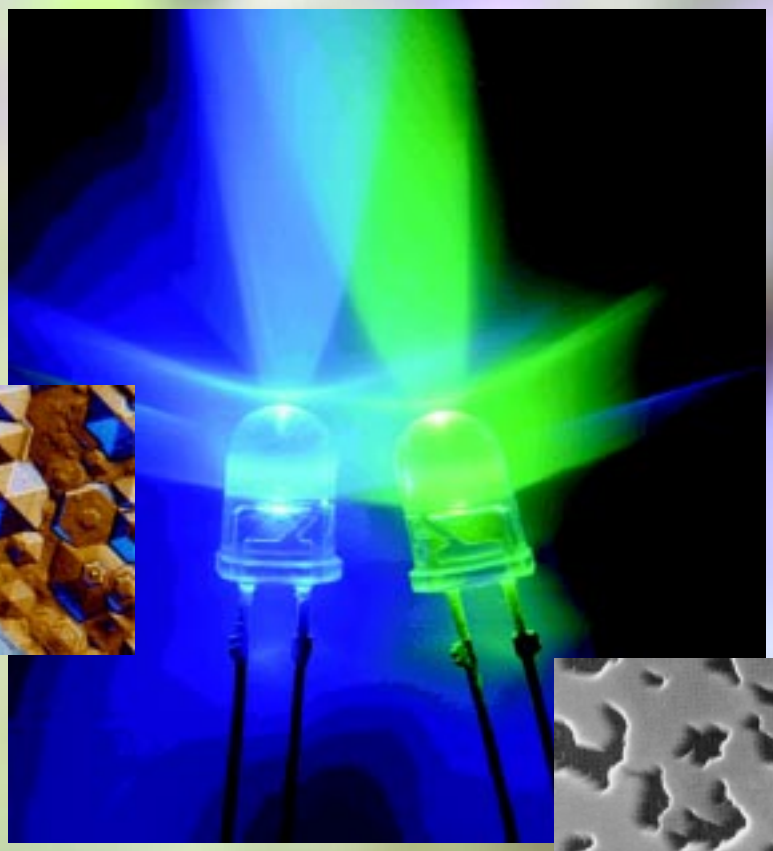
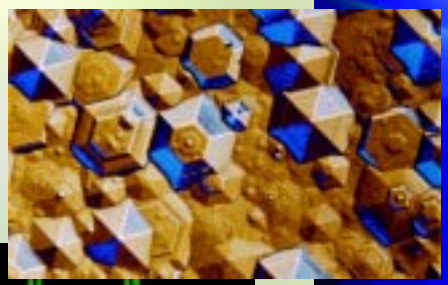
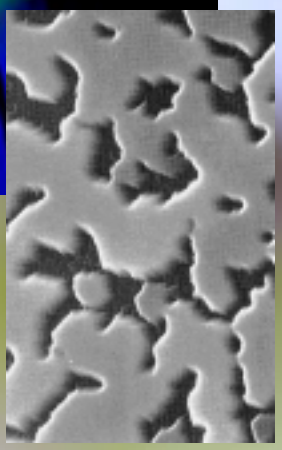
Wide Bandgap Semiconducting Materials and Device Challenges







From the Guest Editor . . .

"Faster, cheaper, smaller" is now the standing order for satellite and probe development at the National Aeronautics and Space Administration.

If only life were that simple for Department of Defense research and development. Although we prefer "more affordable" to "cheaper," comparatives such as "lighter," "more powerful," "more efficient," "broader band," "higher frequency," "lower noise," "stealthier," and "higher resolution" abound in the modern Navy's research, development, and engineering (RD&E) lexicon. Defense electronics RD&E does not pass muster unless it fits these, and many more, criteria.

In truth, we in the DoD should use mostly superlatives, e.g., *most* efficient, for that is what we mean: only the best is good enough for the U.S. military. ONR's function is to ensure that the best is what they get.

More than 80% of command, control, communications, computers, and intelligence (C4I) system electronics performance is achieved with silicon (Si; specifically, complementary metal-oxide on silicon (CMOS)). Similarly, the highest performance microwave, millimeter wave, and opto-electronic functions depend upon cubic III-V semiconductors: GaAs, InP, and their alloys with AlAs, etc. Development, perfection, and insertion of these compounds were largely the results of ONR's (especially Max N. Yoder's) forward thinking and oversight, and of sustained investment by ONR and DARPA over the last 30 years.

For more than 20 years, Max N. Yoder has been pushing the wide bandgap boat out into a very skeptical sea. Although the true potential of wide bandgap semiconductors such as GaN and SiC was recognized more than 50 years ago, until recently the materials problems were thought insurmountable. Multifunction electromagnetic systems under development require electronics performance that can only be delivered by wide bandgap semiconductors.

What is it about these newer semiconductors that makes them so necessary and attractive? Large bandgaps mean that leakage and avalanche onset by generation-recombination currents are insignificant at normal temperatures. With three-to-tenfold higher thermal conductivities, heat dissipation is more efficient, and dielectric constants are approximately 30% lower, thereby reducing parasitic capacitances. Most importantly, however, is that breakdown voltages are an order of magnitude higher, allowing higher voltage swings.

Before these properties can be exploited, however, several challenges remain to be solved in the area of materials.

- Silicon carbide (SiC), although it can be grown in bulk crystals at atmospheric pressure, requires enormous temperatures, which in turn limits the size of crystals and leads to many large defects, known as micropipes.
- GaN bulk growth is not yet a reality, owing to the enormous rate of decomposition above 1,000 °C. Other potential solutions, such as compliant substrates, lateral growth, and pendeo-epitaxial overgrowth (that is, epitaxy sideways over a substrate, which reduces defect density by five orders of magnitude) are under ONR-funded investigation.
- Acceptor dopants are "deep" in SiC, deeper still in GaN, and too deep in AlN. Thus, such components as lasers and bipolar transistors, which depend on low resistivity *p*-type films, are most challenging to produce. Solutions to this particular challenge may come from recent ONR initiatives in spontaneous and piezo-polarization-induced hole conduction.

World experts address these and other related wide bandgap materials and device challenges in this edition of *Naval Research Reviews*.

Colin Wood
Office of Naval Research

Cover: Photograph of blue and blue/green LEDs courtesy of Cree Research, Inc.

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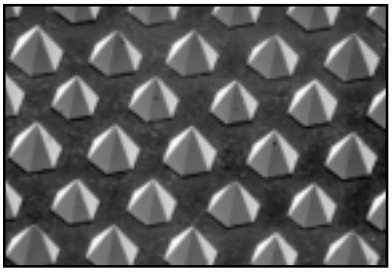

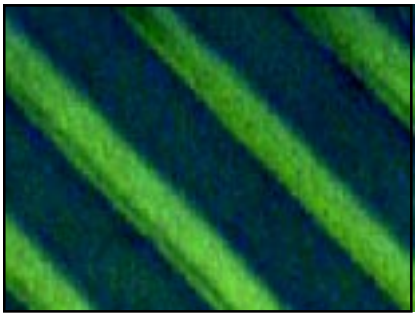


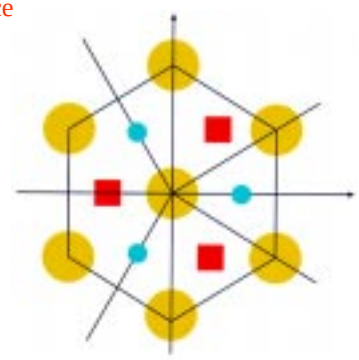

The Compound with Many Faces

On the technological stage, silicon carbide (SiC) has in the last 50 years moved from its previous supporting actor roles in the dramas of the early 20th Century Industrial Age into the spotlight of the Technological Age thrillers now being cast for the new millennium. Although this naturally occurring compound has probably existed since before our solar system was born, it has truly come into its own only in the last 10 years. Its over 170 polytypes, each with its own unique optical and electronic properties, make this material a versatile leading actor in the power semiconductor theater. SiC, with its wide bandgap, has much higher thermal conductivity and much higher electrical breakdown than Si, which means that it is ideal for smaller structures that dissipate more power. That's the charm for power applications: smaller structures mean faster switching rates. In fact, while Si devices shut down slowly in a ping-ponging on-off process, SiC devices do not do that, and are therefore four to five times more efficient. That yields energy savings that are big box office for high power applications.

Professors W.J. Choyke and Robert P. Devaty of the University of Pittsburgh explore the material science behind this compound's road to stardom. Along the way, they review its history, explain polytypism, and describe SiC's band structures, lattice vibrations, and impurity and defect states. It's a standing ovation for this comeback star.

– S.O.

SiC — The Power Semiconductor for the 21st Century: A Materials Perspective

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Introduction

Isn't it ironic that silicon carbide (SiC), by far the oldest of the compound semiconductors, has had to wait until the 21st Century to realize its great promise? Astrophysicists discovered during the last 25 years that grains of material that formed around stars other than our Sun *before* our solar system was born 4.6 billion years ago have actually managed to reach our planet. Perhaps the best studied of these grains is SiC! Most of this SiC is believed to have originated around stars on the asymptotic giant branch, whereas a small fraction of it can be traced to ejecta from supernova.

History

The first hint that there could even be a bond between carbon and silicon was first enunciated by the great Swedish chemist Jöns Jakob Berzelius in 1824. Sixty-seven years later in Monongahela, Pennsylvania (near present-day Pittsburgh), Eugene G. Acheson melted a mass of carbon and aluminum silicate by passing a high current through a carbon rod immersed in this mixture. After the mixture had cooled to room temperature, Acheson found small, bright blue crystals in the vicinity of the carbon rod. He fully expected to have made a compound of aluminum and carbon, and since Al_2O_3 had been called *corundum*, he named his "new" compound *carborundum.* Acheson had an excellent chemist on his staff who very quickly determined that the composition of this "new" compound was in reality 70% silicon and 30% carbon by weight. It was the compound SiC whose existence was first hinted at by Berzelius. For reasons that defy logic, SiC nevertheless became known as *Carborundum*™ the world over.

Acheson was quick to send some of his new SiC crystals to Professor B.W. Frazier at Lehigh University in Bethlehem, Pennsylvania. Frazier was a gifted crystallographer, and he quickly determined by means of optical goniometry that Acheson's SiC crystals came in many crystallographic structures called *polytypes*. To date, over 170 polytypes of SiC have been discovered. Since polytypism radically influences the properties of SiC, we will now spend a little time analyzing the nature of polytypism in SiC.

What are Polytypes?

Let us consider Fig. 1 where we designate a Si-C atom pair in an A-plane double layer in close packing as Aa, in the B plane as Bb, and in the C plane as Cc. It is possible then to generate a series of structures by varying the stacking

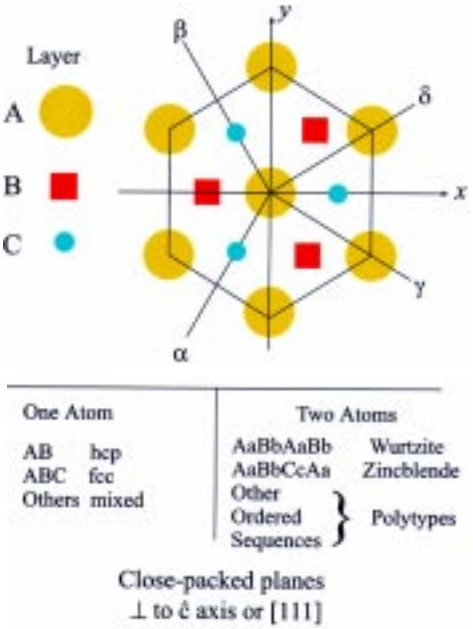


Fig. 1 - Close-packed planes perpendicular to the c axis (principal axis) in hexagonal or rhombohedral lattices or [111] in diamond or zincblende lattices. Note that the z axis, mentioned in the text, is perpendicular to the x-y plane.

sequence along the principal crystal axis (the z axis, perpendicular to the x and y axes in Fig.1). For **AaBbCc** AaBbCc…stacking, we generate the zincblende (cubic) form of SiC known as 3C-SiC. On the other hand, if we stack the atom pairs as **AaBb**AaBb…we generate the wurtzite (hexagonal) form of SiC known as 2H-SiC. Other common forms of SiC may be generated by the following stacking sequences along the principal axis: 4H-SiC (**AaBbAaCc**AaBbAaCc…), 6H-SiC(**AaBbCcAaCcBb** AaBbCcAaCcBb…) and 15R-SiC(**AaBbCcAaCcBbCc AaBbAaCcAaBbCcBb**AaBbCcAaCcBbCcAaBbAaCcAa BbCcBb…). The notation is clear: **C** for cubic, **H** for hexagonal, and **R** for rhombohedral. For simplicity, when dealing with SiC, one normally reduces the notation **Aa, Bb, Cc** to **A, B, C**. It is interesting to note that the largest unit cell of a SiC polytype that has thus far been identified has an astounding length of about 1200 Å along the principal axis (the z axis, also commonly referred to as the c axis). The reason for the stability of so many SiC polytypes is still a question of great interest and current study.

The long slender unit cells of SiC are not just a scientific curiosity but are in fact the reason that we should think of SiC as a large family of semiconductors. Each polytype of SiC has some unique optical and electronic properties. The designer of a particular SiC device should consider very carefully in which polytype optimum characteristics may be obtained. One reason for this diversity is that the number of inequivalent Si or C sublattice sites varies among the polytypes. For example, there is one in 3C and 2H, two in 4H, three in 6H, and five in 15R. This means that if we substitute nitrogen (N), which acts as a donor in SiC, or aluminum (Al), which acts as an acceptor in SiC, in the 4H lattice, we obtain not just one donor/acceptor but rather *two* donors/acceptors. In 6H-SiC, we would have *three* donors/acceptors, and in 15R SiC, *five* donors/acceptors. Why is this so? Figure 2 is a schematic representation of the atomic arrangements of the Si and C atoms in the $(11\bar{2}0)$ plane of the 6H-SiC hexagonal pyramid. In general, when representing the atomic stacking of any SiC polytype in the $(11\bar{2}0)$ plane, the complicated stacking sequences can be expressed in terms of simple zigzags. As shown in Fig. 2, 6H-SiC can be illustrated by a zig of three lattice positions (ABCA) to the right and a zag of three lattice positions to the left (ACBA). In short hand, we write (22) for 4H, (33) for 6H, and (232323) for 15R, and so on.

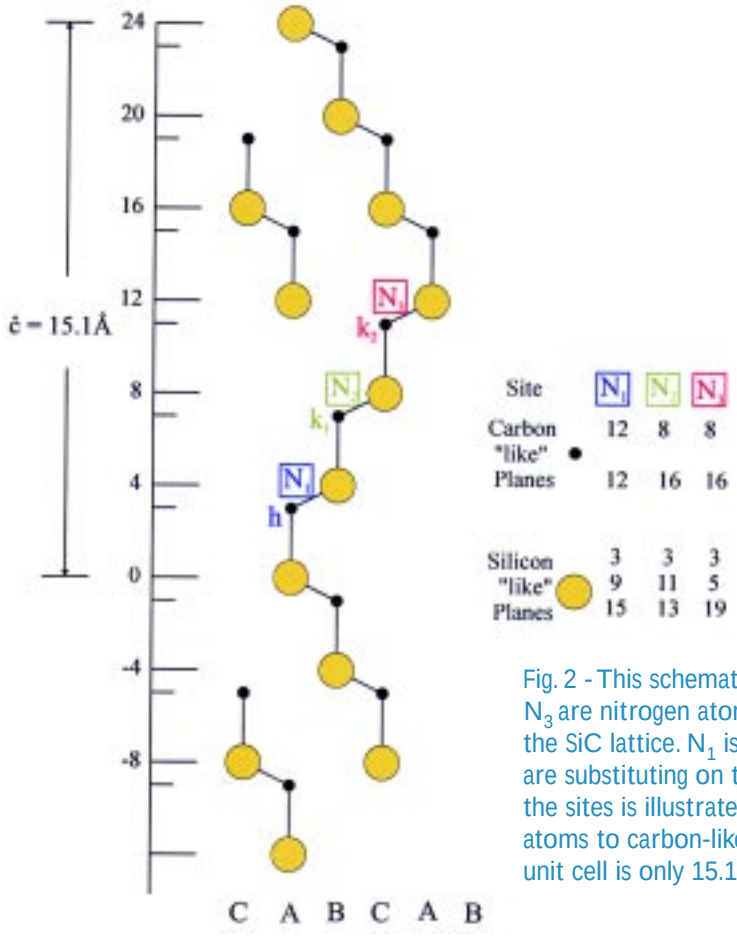


Fig. 2 - This schematic illustrates inequivalent sites in 6H-SiC. N_1, N_2, and N_3 are nitrogen atoms substituting on three inequivalent carbon sites in the SiC lattice. N_1 is substituting on a hexagonal site, **h**, and N_2 and N_3 are substituting on two quasicubic sites, $\mathbf{k}_1$ and $\mathbf{k}_2$. The inequivalence of the sites is illustrated in the table by the distance of each of the nitrogen atoms to carbon-like and silicon-like planes. Note that the length of the unit cell is only 15.1 Å as indicated on the left of the figure.

Looking more carefully at Fig. 2, we designate a carbon atom on a particular plane perpendicular to the c axis with a small dot and the associated silicon atom with a larger gold circle. A point **h** designates a lattice position in which the carbon or associated silicon atom finds itself in a "quasihexagonal" stacking environment with respect to its neighboring stacking planes. Similarly, we see that $\mathbf{k}_1$ and $\mathbf{k}_2$ represent lattice points in which the carbon and associated silicon atoms find themselves in "quasicubic" stacking environments. In addition, as the inset shows, if we substitute a nitrogen atom at the **h**, $\mathbf{k}_1$, and $\mathbf{k}_2$ carbon sites, the atomic distances for the substitutional N_1 nitrogen to the nearest carbon-like or silicon-like planes distinctly differ from those for the substitutional N_2 and N_3 nitrogen atoms. The N_2 and N_3 nitrogen atoms sense different environments! This shows why the hexagonal site **h** and the two cubic sites $\mathbf{k}_1$ and $\mathbf{k}_2$ in 6H-SiC are expected to have, and do have, slightly different electronic properties.

Figure 3 shows the stacking sequences and selected physical properties of the five polytypes of major interest to current research and development. The lattice constant in the zincblende 3C-SiC modification and the lengths of both the pyramid face and the principal axes of the unit cells in the case of the hexagonal lattices for 15R, 6H, 4H, and 2H-SiC are all obtained from X-ray measurements. Once the unit cells for the various polytypes are known, the number of atoms per unit cell is determined as well as the number of inequivalent sites. The space groups for the various polytypes are a consequence of the atomic arrangements of the Si and C atoms in each polytype. Finally, the indirect exciton energy gap at 2K is obtained from optical measurements. The latter leads us directly, in the following section, into a consideration of the band structure of SiC polytypes.

Band Structure

During this decade, much progress has been made by theorists in elucidating the electronic and vibrational structure of the polytypes of SiC, some of whose physical properties are shown in Fig. 3. At the same time, improved crystal quality and purity have made experiments possible to verify the theory and point to new directions that require a great deal more study. It has been known since the late 1950s that SiC is an indirect semiconductor. To illustrate what we mean, refer to Fig. 4. This is a schematic represen-

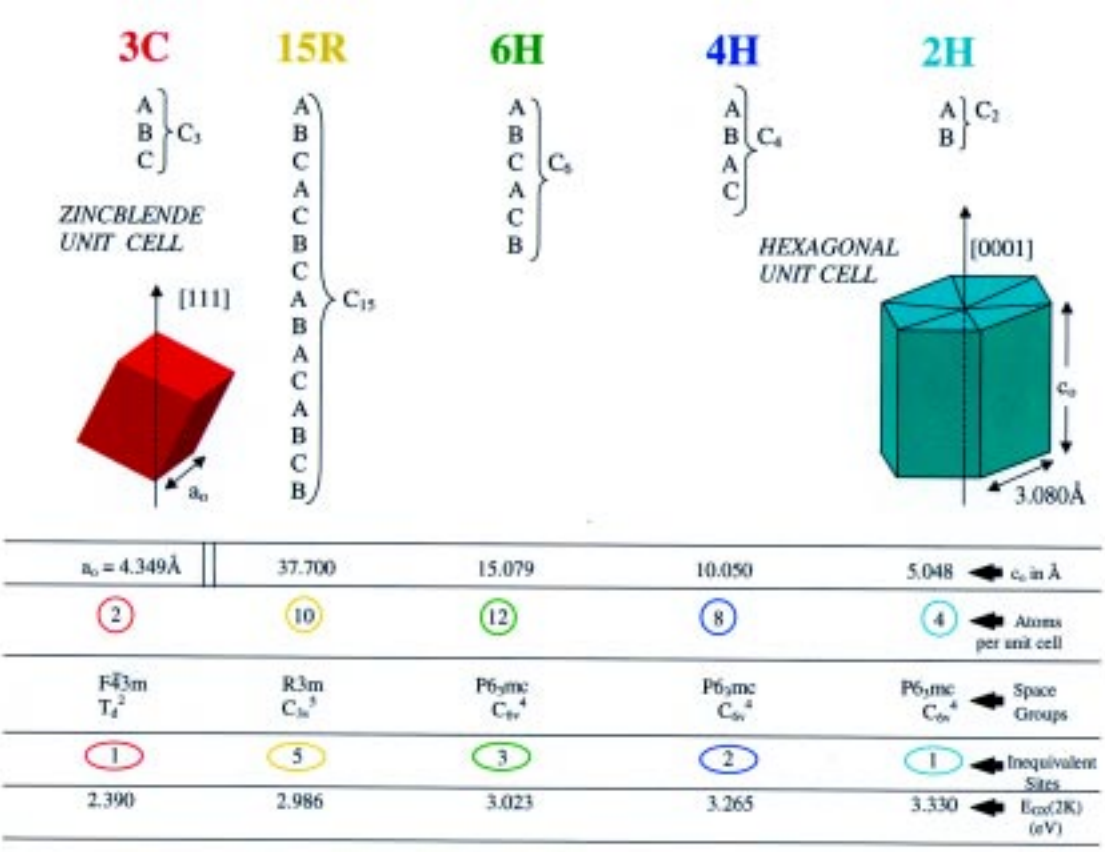


Fig. 3 - A summary of some of the physical properties of 3C, 15R, 6H, 4H, and 2H-SiC. If these polytypes are all represented in the $(11\bar{2}0)$ plane of a hexagonal pyramid, then the repeat distance along the c axis would be c_n.

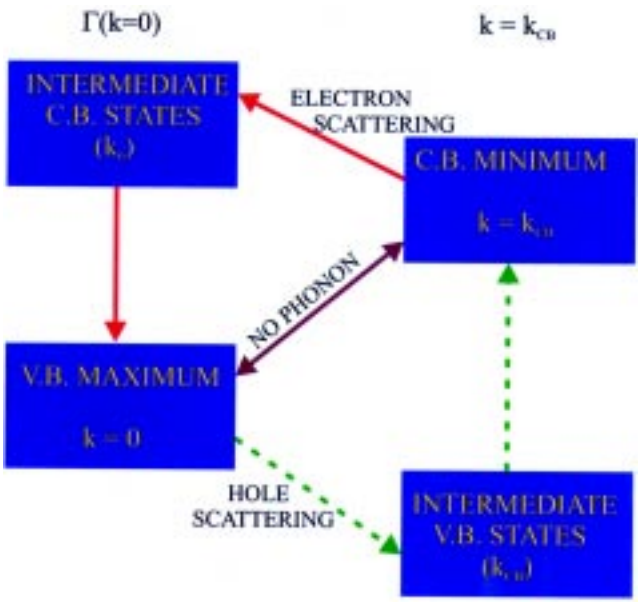


Fig. 4 - An illustration of possible electronic transitions from the maximum of the valence band to the minimum of the conduction band.

tation of indirect exciton recombination for a semiconductor with the valence band (VB) maximum at **k** = 0 and conduction band (CB) minima at **k** = $\mathbf{k}_{CB}$. In a direct semiconductor such as GaAs or GaN, the extrema of the valence and conduction bands are located in the same place in **k** space at the center of the Brillouin zone, the Γ point, and the absorption or emission of photons can take place without the assistance of lattice phonons. We term such transitions *direct*. In SiC, Si, and Ge, the CB minima are not at the same place in **k** space as the VB maximum and we require the extra help of phonons to permit transitions from the VB to the CB. Such transitions are termed *indirect*. As Fig. 4 shows, there are various possibilities for making these transitions. One could either scatter an electron with a phonon from the CB minimum to an intermediate state at $\mathbf{k}_0$ (**k** = 0) in the CB and then make a direct transition to the VB maximum or one can scatter a hole via a phonon to an intermediate state in the VB at $\mathbf{k}_{CB}$ and then make a direct transition to the CB minimum.

Most experimental information about the band structure of SiC has come from low-temperature optical experiments. Near zero degrees Kelvin, if one absorbs a photon with energy larger than the bandgap and raises an electron from the VB to the CB, leaving behind a hole in the VB, one has created an excited state of the crystal. After a very short time, the free electron in the CB as well as the free hole in the VB not only scatter to the minimum of the CB and maximum of the VB, respectively, but lower their energy even further by having a slight coulomb attraction for each other. We call such an electron-hole pair a *free exciton*. In low-temperature experiments, in which we attempt to determine the bandgaps of the polytypes, we really measure the energy that it takes to overcome the bandgap minus the energy that is given back due to the slight coulomb binding of the electron-hole pair (exciton). Hence, we measure the exciton bandgap (E_{GX}) values that were given in Fig. 3. We now need to explain the existence of the "no-phonon" transition indicated in Fig. 4. If we have impurities or defects that have energy levels in the bandgap, it is very probable at low temperatures that the exciton is captured and bound to these centers. This localization permits a small number of transitions to the VB to proceed without the need of phonon participation. In the case of low-temperature photoluminescence (LTPL), we indeed see very sharp no-phonon lines and they are immensely helpful in the analysis of the data.

A comprehensive treatment of the fundamental theoretical aspects of SiC has recently been given in the first six articles in "*Silicon Carbide:…Vols. I and II*" [1]. One is struck by the progress that has been made since the start of the current renaissance of SiC in the late 1980s. Of particular interest for device development is the guide that theory has given in locating the positions of the conduction band minima in the zincblende Brillouin zone of 3C-SiC, in the hexagonal Brillouin zones of 2H, 4H, and 6H-SiC, and in the rhombohedral Brillouin zone of 15R-SiC. Theory has also given valuable guidance as to the structure of the VB near its maximum at **k** = 0 in several of the common polytypes. Finally, theory has made great strides in calculating the tensor components of the electron-effective masses in the common polytypes of SiC. The hole effective masses have also been estimated but there is unfortunately no experimental confirmation available to date.

Figure 5 summarizes the best current information from experiment and theory concerning the CB minima as well as the VB maxima for 2H, 4H, 15R, 6H, and 3C-SiC. Numerical values obtained purely from theory are marked as such. We have arranged the polytypes with the 2H wurtzite structure at the top and the zincblende 3C structure at the bottom. This ordering in terms of "hexagonality" shows a number of interesting trends. As we go from 2H to 3C-SiC, the forbidden gap becomes progressively smaller. Lambrecht et al. [2] have shown how this comes to pass from their band theoretical considerations. At the top of the VB, there is a threefold degeneracy (neglecting spin) and we expect the spin-orbit interaction ($\Delta_{S\text{-}O}$) in the cubic,

Polytype	Hexagonality	Exciton Bandgap E_{GX} (2K)	Position of Conduction Band Minimum in the Brillouin Zone	# of CB minima	Δ_{S-O} (meV)	Δ_{C-F} (meV)
2H	1	3.330	K (HEXAGONAL)	2	—	144 (Theory)
4H	0.5	3.265	M (HEXAGONAL)	3	—	72 (Theory)
15R	0.4	2.986	X (RHOMBOHEDRAL)	3	7	57 (Theory)
6H	0.33	3.023	U (L - M) HEXAGONAL	6	7	44
3C	0	2.390	X (ZINCBLENDE)	3	10	0

Fig. 5 - A compilation of salient features of the band structures of 2H, 4H, 15R, 6H, and 3C-SiC.

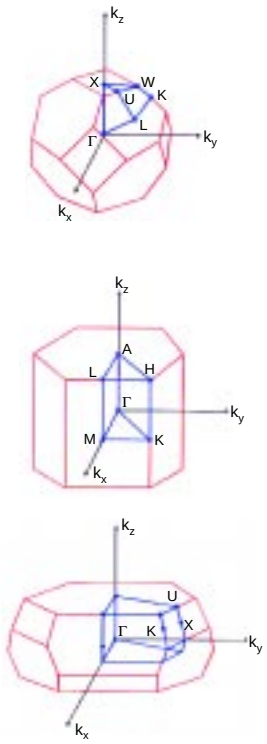
zincblende, lattice to split this degeneracy into fourfold and twofold degenerate bands at **k** = 0. For the hexagonal and rhombohedral polytypes, we have in addition a crystal field that results in an additional splitting (Δ_{C-F}) such that we have three nondegenerate bands at the VB maximum at **k** = 0. We see from Fig. 5 that in the hexagonal and rhombohedral polytypes, we measure a spin-orbit splitting of about seven milli-electron-volts (meV), whereas in the cubic modification 3C-SiC, we find a spin-orbit splitting of 10 meV [3, 4]. Theory [2] predicts a linear crystal-field splitting from zero to 144 meV as we go from cubic SiC (3C-SiC) to 100% hexagonal SiC (2H-SiC). Until now, we have only been able to measure the crystal-field splitting in 6H-SiC [5], and the experimental value of 44 meV is in good agreement with the value expected from theory.

Band calculations are used by several authors, in slightly different approaches, to obtain the effective mass tensor components for the bottoms of the conduction bands in the polytypes under discussion. A knowledge of the electron effective masses is extremely important for device modeling. Various optical techniques as well as cyclotron resonance have been used to obtain electron effective mass values in 3C-SiC. Here the various experimental techniques are in excellent agreement. Except for 4H-SiC, for which optical detection of cyclotron resonance has given reliable values of the electron effective mass tensor components, we have run up against serious interpretational problems in absorption experiments on shallow donors, mainly due to a lack of a proper and sufficiently general effective mass theory. Figure 6 is an adaptation from a table in the paper of Wellenhofer and Rössler [6] where all the current experimental and theoretical values for the effective mass components at the respective CB minima for 3C, 2H, 4H, 6H, and 15R-SiC are given. For clarity we have left out the references to the various calculations and experiments, but all the references may be found in Wellenhofer and Rössler [6]. As one of our next important tasks, it will be most useful to get accurate and reliable measurements of all the band parameters in the pure wurtzite 2H form of SiC. The simplicity of the 2H modification will facilitate further intrepretation in the more complicated hexagonal and rhombohedral polytypes. Unfortunately, this will require much larger, less defective, and much purer single crystals of the 2H polytype, presenting a super challenge to the crystal growers!

Lattice Vibrations

We have already mentioned that in LTPL, many sharp lines are observed, most of which result from transitions involving phonons (lattice vibrations). These experiments are a rich source of information on phonons, especially in indirect semiconductors such as SiC. However, the phonons that we see in these spectra are characteristic of very special positions in **k** space. In spectra due to free excitons or excitons bound to shallow donors, we sense the phonons characteristic of the **k** space positions of the CB minima in 2H, 4H, 6H, 15R, and 3C-SiC.

Other common techniques for the study of vibrational properties in semiconductors are Raman scattering and neutron scattering. Until very recently, no single crystals of SiC of sufficient size have been available to make neutron scattering practical. In 1968, Feldman, Parker, Choyke, and Patrick [7, 8] introduced a new method of using Raman scattering to obtain phonon dispersion curves based on the existence of polytypes. Measurements on a polytype often yield results that are determined partly by the properties



m(m_0)		THEORY				EXPERIMENT			
3C SiC		minimum at X							
$m_{\|\|}$	0.70	0.67	0.63	0.68	0.60	0.667	0.67	0.67	
$m_{\perp}$	0.23	0.25	0.23	0.23	0.29	0.247	0.25	0.22	
2H SiC		minimum at K							
$m_{\perp}$	0.40	0.45	0.45	0.43					
$m_{\|\|}$	0.26	0.26	0.27	0.26					
4H SiC		minimum at M							
$m_{M\text{-}\Gamma}$	0.66	0.57	0.58	0.57		0.58	$m_{\perp}$: 0.18	0.30	
$m_{M\text{-}K}$	0.31	0.32	0.28	0.28		0.31			
$m_{M\text{-}L}$	0.30	0.32	0.31	0.31		0.33	$m_{\|\|}$: 0.22	0.48	
6H SiC		minimum along M-L							
$m_{M\text{-}\Gamma}$	0.78	0.75	0.77	0.75		$m_{\perp}$: 0.35	0.24	0.25	0.42
$m_{M\text{-}K}$	0.23	0.27	0.24	0.24					
$m_{M\text{-}L}$	1.2-2.0	1.95	1.24	1.83		$m_{\|\|}$: 1.4	0.34	1.7	2.0
15R SiC		minimum at X							
$m_{X\text{-}\Gamma}$	0.67					$m_{\perp}$: 0.28	0.24		
$m_{X\text{-}K}$	0.22								
$m_{X\text{-}U}$	0.41					$m_{\|\|}$: 0.53	0.38		

Fig. 6 - Theoretical and experimental values for the effective electron masses in 3C, 2H, 4H, 6H, and 15R SiC. The different columns compare different theoretical as well as experimental values obtained in a variety of ways.

common to all polytypes and partly by the unique structure of the polytype on which the measurements are made. An example is the first-order Raman spectrum of 6H-SiC [7]. The property assumed to be common to all polytypes is, in this case, the phonon spectrum in the axial direction [8]. Most of the lines in the Raman spectrum are, nevertheless, characteristic of the 6H-SiC structure, which determines the points of the common dispersion relation spectrum accessible to Raman measurements. The relationship of the Raman spectrum to the phonon spectrum is clear from a large zone [9] point of view, which permits the assignment of Raman frequencies to positions on dispersion curves, even though these modes have zero wave vector (approximately) in the Brillouin zone. The procedure is now termed "zone folding" and is used extensively in the analysis of data obtained from semiconductor superlattices grown by means of molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) techniques. Figure 7 illustrates the existence of a common SiC phonon spectrum (within ~2%) for polytypes 4H, 6H, 15R, and 21R-SiC. Nakashima et al. [10] have added data for 8H and 27R-SiC, which fit extremely well on the curves shown in Fig. 7. This method has given us phonon dispersion curves comparable in completeness and accuracy with those obtained for other materials by neutron diffraction (but only for one direction in momentum space). Nakashima and Harima [11] have recently given a detailed review of the current applications of Raman scattering to the study of the vibrational properties of the polytypes of SiC.

Impurity and Defect States

In a perfectly ideal world, we would first produce ultrapure single crystals of a material before attempting any doping with impurities. Fifty years ago we already knew that certain impurities such as nitrogen, aluminum, and boron could be readily incorporated into SiC. We also knew that nitrogen made SiC *n*-type, and aluminum and boron made SiC *p*-type. What we didn't know was how to produce a relatively clean and defect-free single crystal. To make matters worse, the best crystals were small platelets with mixed polytypes. The cry then was, if we could only produce large boules of a single polytype with a high degree of doping control, we would have a marvelous industrial process. These things have now come to pass! Two-inch wafers are rapidly becoming available with a low enough micropipe density to serve most applications. The *n*- and *p*-type doping ranges of these boules can be controlled from roughly 5×10^{15} cm^{-3}

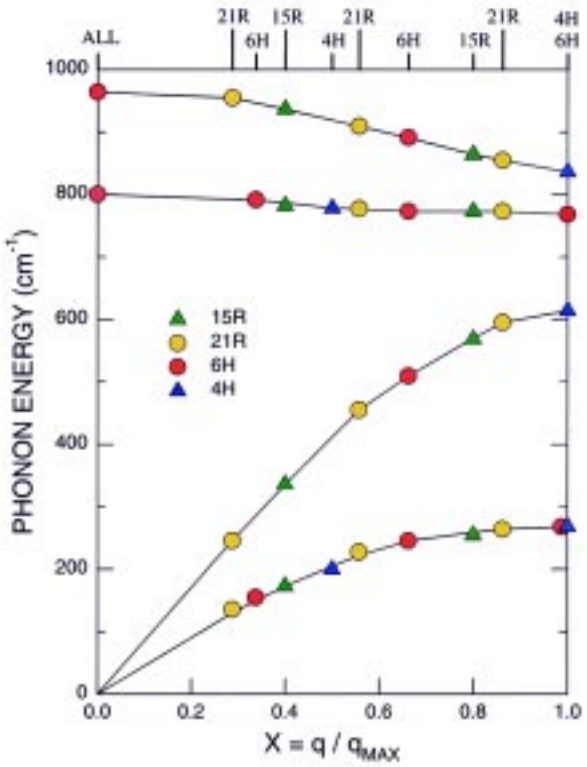


Fig. 7 - A common SiC phonon spectrum (within ~2%) derived from first order Raman scattering data in the polytypes 4H, 6H, 15R, and 21R-SiC.

to 5×10^{19}cm^{-3}. Device structures are presently made on homo-epitaxial films grown on boule wafers. Currently used epitaxial films range from a thickness of about 0.5 μm to 100 μm and a range of possible *n*- and *p*- type doping of less than 10^{14}cm^{-3} to greater than 10^{19}cm^{-3}.

The conductivity type of SiC, as we have already learned, can be adjusted by doping with either donors such as nitrogen and phosphorus or acceptors such as aluminum, boron, or gallium. Most doping must be done during boule or epitaxial growth since the diffusion coefficients for these dopants are very small at workable temperatures. An alternative is ion implantation, which has been used extensively in SiC, although it is far more difficult to use than in a single atom material such as Si. Even at annealing temperatures of 1700 °C, residual defect centers from the implantation may still be present. Understanding and controlling such centers are key to using ion implantation in SiC.

Nitrogen is the best studied donor in SiC. It is known to substitute on the carbon sublattice and some have claimed to achieve doping densities as high as 3×10^{20} cm^{-3}. A very high doping density is required for vertical power device structures to obtain low power losses. Resistivity values of about 2×10^{-3} Ω-cm have been reached in SiC boule wafers, which are used as the substrates for these devices. A resistivity of 2×10^{-3} Ω-cm compares favorably with values that have been reported for Si. For high frequency devices, on the other hand, semi-insulating substrates are desirable. By compensating boules during growth with elements such as vanadium, resistivities of about 10^{9} Ω-cm at 500 K have been reported. Another approach that is appealing and is currently being actively pursued is producing bulk material that is so pure that the intrinsic resistivity is high enough to satisfy the demands of the high frequency designs and at the same time preserve the good transport characteristics of the material. In epitaxial growth, the residual nitrogen concentration is normally the limiting feature in making films with carrier concentrations below 10^{14} cm^{-3}. Very high voltage applications (i.e., greater than 25 kV) are now driving efforts to produce thick single-crystal films (100 μm) with ultra high purity (less than 5×10^{13} dopants per cm^{3}).

In the last few years, phosphorus donors have been incorporated into 6H-SiC during epitaxial growth by ion implantation and through neutron transmutation. Only in the CVD-grown material have we seen a bound exciton spectrum of phosphorus. It gives the signature of a slightly shallower donor than nitrogen. Ionization energies obtained from Hall measurements on implanted and annealed material bear this out. If we invoke site competition epitaxy (SCE) in analyzing the CVD growth, we conclude that the phosphorus substitutes on the Si sublattice. Atomic size arguments and evidence from electron spin resonance (ESR) measurements also point in this direction.

Gallium, aluminum, and boron serve as “shallow” acceptors in SiC and are most frequently introduced during the growth process. However, implantation can be used to generate *p*-type material by overcompensating the nitrogen donor background. Gallium and aluminum substitute on the Si sublattice but the situation for boron appears more complex. Boron is a maverick by forming a shallow acceptor as well as a deep state that acts like an acceptor from the point of view of donor-acceptor recombination spectra. Current interpretations of ESR and electron nuclear double resonance (ENDOR) experiments point to the following: The shallow boron state is due to a boron atom at an offcenter position near a Si sublattice site. The deep center is due to a boron atom at an offcenter position near a Si sublattice site adjacent to a vacancy on the carbon sublattice site. Both the deep and shallow boron centers are aligned along the principal crystal axes. In contrast to the situation with donors, the ionization energies of the acceptors are only weakly dependent on polytype or on the hexagonal (**h**) and

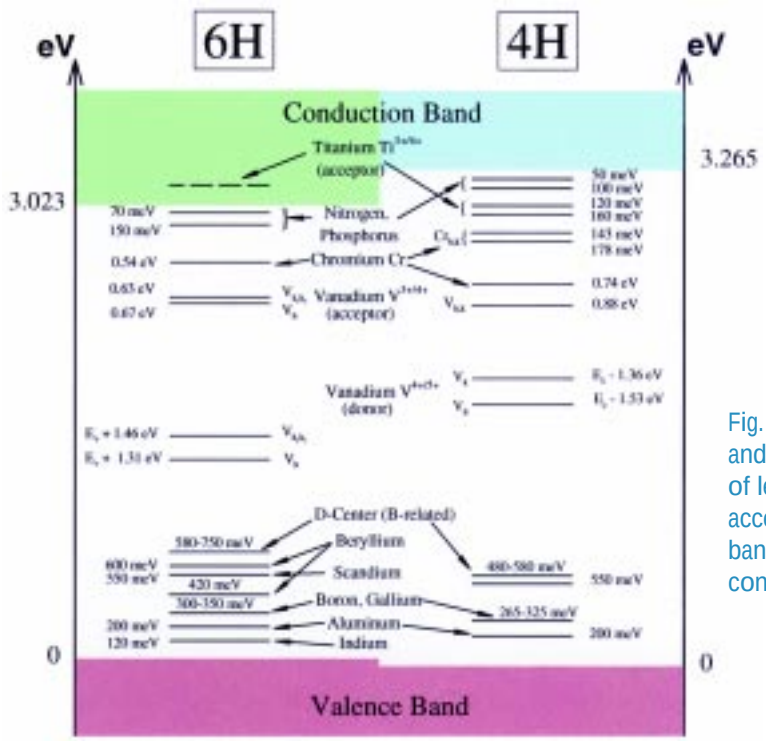


Fig. 8 - Impurity centers in SiC polytypes 6H and 4H. For the sake of clarity, the positions of levels for the various donors and acceptors are not drawn to scale. The valence band offset is taken to be 50 meV, and the conduction band offset is 192 meV.

quasicubic (**k**) lattice sites. Hall measurements yield an average value for the ionization energy of aluminum of about 200 meV, and for the shallow boron acceptor, they yield an average value of the ionization energy of about 300 meV. In CVD growth, the concentrations of shallow and deep boron centers can be adjusted by use of SCE.

Figure 8 is an adaptation of a figure from the recent Ph.D. dissertation of Thomas Troffer at the University of Erlangen-Nürnberg. Here we summarize what is known about the energy levels of the main impurities in SiC. The band offsets between polytypes are believed to occur mainly in the conduction bands. For the VB offset between 6H- and 4H-SiC, we take a value of 50 meV, leaving 192 meV for the 6H- to 4H-SiC CB offset. The large CB offset accounts for the fact that in 4H-SiC, one observes two acceptor levels for $Ti^{3+/4+}$, whereas in 6H-SiC, these levels are resonant with the CB and, hence, are not seen. For the sake of clarity, the energy positions of the donor and acceptor levels in the forbidden gap have not been drawn to scale. Furthermore, the quoted binding energies are rough values and are subject to much fine-tuning!

We have already alluded to the fact that during ion implantation, defect states are introduced into the SiC lattice. Some of these states have been extensively studied. The so-called D_I and D_{II} centers [12] appear to be the most persistent and can still be detected after a 1700 °C anneal. Their effect on electrical properties of SiC is still not certain and is currently under study. High energy electron bombardments (i.e., higher than 1 MeV) have led to annealing studies of lattice defects from room temperature up to 1700 °C. The main conclusions seem to be that up to 800 °C, single vacancies can exist in SiC, whereas above this temperature, only vacancy complexes are stable. During boule and epitaxial growth, some of the same defect centers seen in irradiated materials may also be generated. Normally these centers are seen, primarily by means of LTPL, after too rapid growth or too rapid cooling after growth. In recent years, many deep levels have also been observed with LTPL and deep level transient spectroscopy (DLTS) measurements but have not as yet been identified. The study of defects in SiC is just in its infancy and will be vigorously pursued because of its clear importance to device performance.

Conclusion

We have seen that SiC has emerged in the last 50 years from being a ceramic material used as a universal abrasive, heating element, and reducing agent in metallurgical processes to a semiconductor of great promise for high power, high frequency devices and unique applications in radiation and corrosive environments. To bring all this about will require a continued, aggressive, and coordinated effort

of materials growth, materials characterization, and fundamental understanding.

Acknowledgment

We wish to thank Dr. S.G. Sridhara for his great help in preparing the figures.

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The Authors

For the biography of **W.J. Choyke**, see Profiles in Science on p. 72 and the inside back cover.

After earning a Ph.D. in Physics from Cornell University, **Robert P. Devaty** was a National Research Council (NRC) Associate at the Naval Research Laboratory. He joined the Department of Physics and Astronomy at the University of Pittsburgh in 1984. In the 1980s, he applied far-infrared and infrared techniques to the study of small particles and metal-insulator composite materials under ONR support. After he was promoted to Associate Professor, he changed the focus of his research to optical studies ranging from the ultraviolet to the far-infrared of large bandgap semiconductors, particularly silicon carbide. Together with W.J. Choyke, he participates in a number of international collaborations, including Gerhard Pensl's group at the University of Erlangen-Nürnberg and Peter Déak's theoretical group at the Technical University of Budapest. He is co-editor of the upcoming International Conference on Silicon Carbide and Related Materials (ICSCRM'99).

SiC transit: Gloria mundi!

Perhaps it is an overstatement to say that the way silicon carbide (SiC) semiconductors pass electric current is one of this world's glories, but the compound's increasing role in advancing high power applications may make a little exaggeration excusable. In the following article, Anant Agarwal and other industry and government researchers illuminate the materials science behind this new-old class of semiconductors, especially its 4H-SiC and 6H-SiC polytypes. They also describe the rapid progress in the development of *p-n* diodes and prescribe steps for further development of SiC power devices. The concurrent surge in the development of SiC-based power metal-oxide semiconductor field effect transistors (MOSFETs) is also summarized. They explain problems such as step-bunching and explore the SiC polytypes' strengths and limitations. Finally, the authors introduce a new power switching device configuration, the JFET Controlled Thyristor, and detail its usability for high power applications, such as those found in power plants and scores of Defense-oriented projects. Of particular interest to Defense S&T is the usability of SiC-based devices in the entire range of all-electric tanks, planes, and ships currently being designed.

– S.O.

Silicon carbide was used in this moissanite gemstone. Photograph courtesy of Cree Research, Inc.

SiC Power Devices

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Introduction

Today's power electronic components are predominantly made of silicon (Si). Silicon technology has matured over the last 40 years, however, so that no major increase in power handling capability of these components is expected in the future. This limit can be overcome by the superior electronic properties of silicon carbide, which offers at least a tenfold increase in power handling capability. High-power, high-speed 4H-SiC diodes and switches operating at high temperatures (>350 °C) are expected to play enabling and vital roles in the design of the future concept military hardware. The system level benefits include a large reduction in the size, weight, and cost of the power conditioning system. To ensure reliability and longevity of military electronics, the junction temperature of conventional silicon-based devices is currently limited to the MIL-STD temperature range of -55 °C to 125 °C. High-temperature devices such as the 4H-SiC rectifiers proposed here can be mounted on high-temperature stations such as motors, generators, and energy management systems to improve mobility, survivability, lethality, and fuel economy. These devices will help in the realization of solid state power conditioning and circuit protection systems used for motors, actuators, energy storage, and pulse power systems. The high power *p-i-n* rectifier proposed here will be critical to the development of DC zonal electric power distribution being developed under Power Electronic Building Blocks (PEBBs). These rectifiers may lead to greatly reduced noise and thermal signatures of ships, submarines, tanks, and armored personnel carriers.

SiC Material Properties

This article describes our approach to very-high-power SiC devices for low-frequency switching applications. Reference 1 presents an overall review of SiC electronics. Although more than 170 polytypes of SiC are known, only two (4H-SiC and 6H-SiC) are available commercially. 4H-SiC is preferred over 6H-SiC for most electronics applications because it has a higher and more isotropic electron mobility than 6H-SiC. Table 1 compares some key electronic properties of 4H-SiC to Si and GaAs.

Table 1 - Key Electronic Properties of Si, GaAs, and 4H-SiC

Property	Silicon	GaAs	4H-SiC
Eg (eV)	1.12	1.5	3.25
μ_n (cm^2/Vs)	1400	9200	800
μ_p (cm^2/Vs)	450	400	140
n_i (cm^{-3}) at 300 K	1.5×10^{10}	2.1×10^{6}	5×10^{-9}
v_{nsat} ($\times 10^7$ cm/s)	1.0	1.0	2.0
E_{crit} (MV/cm)	0.25	0.4	3.0
ΘK (W/cmK)	1.5	0.5	4.9

The most important property of SiC from the power device perspective is its indirect bandgap, which results in relatively high recombination lifetime (~1 μs) provided the material is pure enough. This allows the development of high-voltage *p-n* junction diodes and *p-n-p-n* thyristors that cannot be produced from a direct bandgap material such as GaN. The higher bandgap of 4H-SiC results in a very high intrinsic temperature of 1650 °C for an extrinsic doping of 10^{16} cm^{-3}. Another advantage of high bandgap is negligible junction leakage currents up to 500 °C (μn_i). This allows high-temperature operation without excessive leakage current or thermal runaway. The high junction temperature increases the heat flux that can be removed from the device,

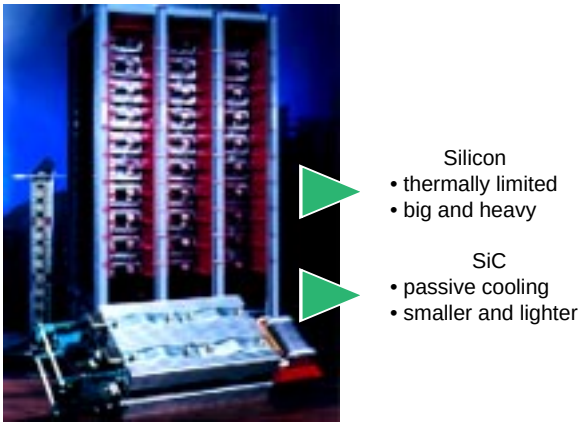
* Currently with Cree Research, Inc., Durham, NC

resulting in reduced cooling requirements. The high breakdown strength, $E_{crit,}$ results in drift layers that are 10 times smaller than those of Si for a given blocking voltage, thus reducing both the storage of minority carriers (i.e., Q_{rr} in diodes is reduced) and associated switching losses at a given switching frequency. This means that the switching frequency can be increased to between 50 and 100 kHz with acceptable switching losses, which, then, would significantly reduce the size and weight of the magnetic components in an inverter system.

Finally, the thermal impedance of the packages is reduced by the high thermal conductivity of SiC, which helps in spreading the heat laterally. It is expected that the size and weight of power electronics using SiC switching devices and diodes will be significantly reduced by means of passive cooling, use of smaller and lighter magnetic components, and reduced snubber size.

SNUBBER. Passive circuit made of resistors and capacitors. They are attached to switches to safeguard them from extreme voltage or current stress during switching events.

Figure 1 shows a three-phase 36-kV transfer switch composed of 10 4.5-kV silicon thyristors in series in each of the three phases. This transfer switch is manufactured by Silicon Power Corporation (SPCO) of Melvern, Pennsylvania and is used by big industrial plants to redirect power from one grid to the other during power failures and other such events. Each thyristor is mounted on a very big heat sink and comes with its own gate-drive circuitry. The high weight, large volume, high cost, and transportation of this unit all present big problems. In a future implementation of SiC technology, each bank of thyristors could be replaced by a single SiC thyristor of 40 kV rating operating at 300 °C on a smaller heat sink, thus reducing the weight, volume, and cost of the system while improving the reliability.



3-Phase Transfer Switch - courtesy of SPCO

Fig. 1 - A 36-kV three-phase transfer switch with 10 silicon thyristors in series in each of the three banks (photo courtesy of Silicon Power Corporation).

p-n Diodes

Virtually all power converter applications require a switch (such as a MOSFET, insulated gate bipolar transistor (IGBT), thyristor, or MOS controlled thyristor (MCT)) and a diode in shunt with it. The transistor is switched on and off at a high frequency (2 to 10 kHz). Increasing the switching frequency can reduce the size, volume, weight, and cost of transformers and inductors in the system but will also increase the switching losses. Figure 2 presents an example of the switching loss in which the current voltage waveform of a diode is shown. As the diode is turned off, a negative spike in current results in high switching losses because the voltage across the diode rises to a high value. The charge released during the negative current spike is known as the reverse recovery charge, Q_{rr}. This represents a big loss component in present-day silicon diodes above 2000 V. Due to the material properties of SiC (particularly its high breakdown field strength), the reverse recovery charge can be reduced by about 90% in SiC diodes.

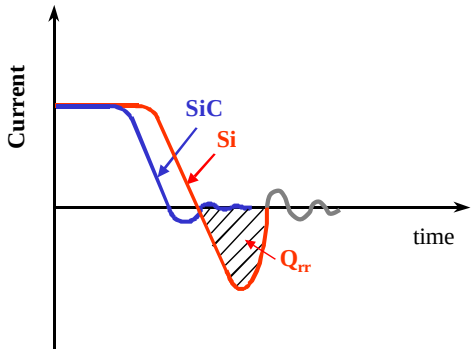


Fig. 2 - Silicon diodes above 2000 V have a large reverse recovery charge, which increases the switching losses. SiC diodes will virtually eliminate it.

Figure 3 illustrates SiC *p-n* diode construction. The diodes are fabricated on n^+ 4H-SiC wafers with 8 to 10 µm of *n*-type epitaxial layers doped at about 5×10^{15} cm^{-3}. Unlike in silicon, foreign atoms do not diffuse in SiC below 2000 °C. Thus, impurity atoms are implanted using high-energy (400 keV) acceleration equipment called ion-implanters. The anode and guard rings are formed by ion-implantation of Al at 1000 °C to the depth of about 0.5 µm with a peak chemical concentration of about 1×10^{20} cm^{-3} using a boxlike profile. The implants are electrically activated at 1700 °C for 10 min in Ar ambient. A sintered titanium layer forms the contact to the p^+ region, whereas sintered nickel is used to contact the backside.

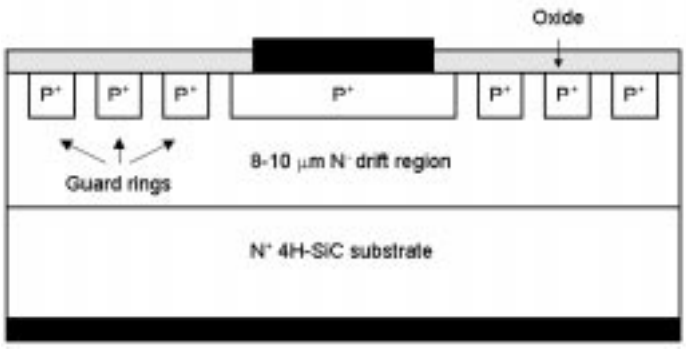
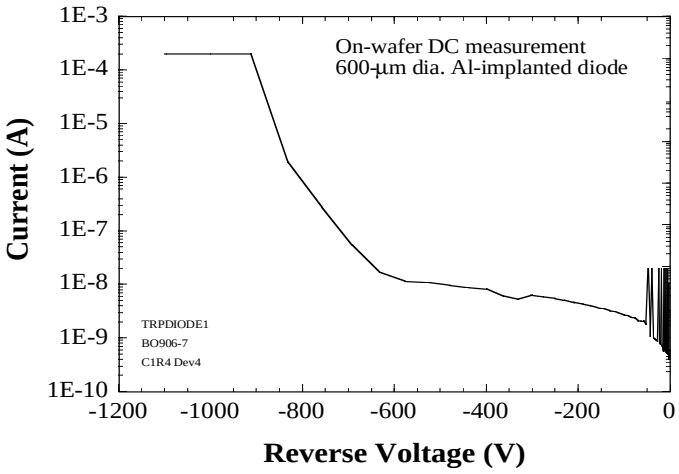


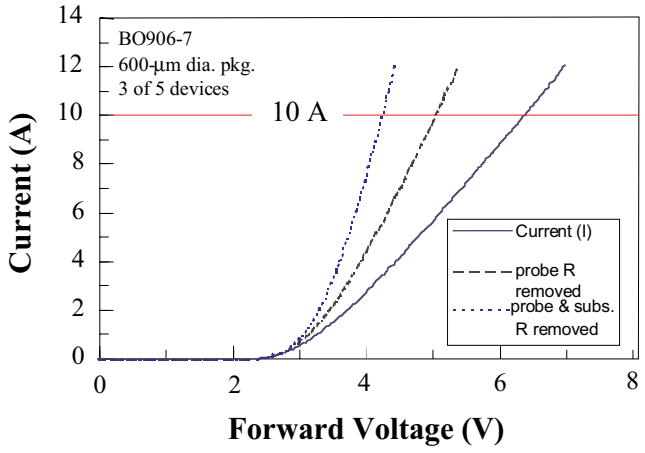
Fig. 3 - A schematic cross section of an SiC implanted diode structure.

The reverse breakdown voltages on diodes of different sizes (100-μm to 1-μm diameter) were measured. The average value of the breakdown voltage was found to be dependent on the size of the diode. For example, the 600-μm diameter diodes broke down at voltages that were typically 20% to 30% lower than the average values for 100-μm diodes. This perimeter- or area-related effect indicates a high dislocation density (low 10^4 cm^{-2}) in the material. The reverse leakage current vs reverse voltage plot (Fig. 4(a)) shows a low leakage current up to about 600 V and then a significant increase up to the breakdown voltage of about 880 V. This also indicates a trap or dislocation-related tunneling process under high electric fields.

The room temperature forward I-V curve for the same diode (Fig. 4(b)) shows high forward drop of 6.5 V at 10 A. The forward drop consists of drops across anode contact resistance, drop across probe and lead resistance, drop in the drift layer, and a drop in the substrate including the backside contact resistance. The substrates are typically 300 μm thick with resistivity of about 0.03 ohm-cm (at room temperature), representing a drop of about 0.45 V at a current density of 500 A/cm^2. A large fraction of the forward drop arises from the poor contact resistance (~ 10^{-3} ohm-cm^2) of sintered Ti to the implanted p^+ regions. This issue is being addressed through coimplantation of C and Al, which has a potential for better electrical activation.



(a)



(b)

Fig. 4 - (a) Reverse and (b) forward I-V characteristics of a 600-μm diameter *p-n* diode.

A Four-Terminal Switch

In addition to a diode, most of the power electronic applications require a switch. Many switches, such as the MOSFET, IGBT, GTO, MTO, and MCT, have been developed using silicon technology. Recent development of a hybrid MOSFET Turn-Off Thyristor (MTO) has been very successful in very high power applications requiring switching of more than both 4000 V and 100 A. In the center of a silicon MTO (Fig. 5) is a silicon Gate Turn-Off

Thyristor (GTO) capable of switching up to 4.5 kV and several hundred amps. Ten MOSFET chips are attached to the periphery of the GTO between the gate and the cathode terminals of the GTO. The MOSFETs are used to help turn the GTO off after it has been turned on. This approach works well for silicon devices but needs to be slightly modified for SiC because the silicon and SiC MOSFETs are not expected to be reliable at temperatures above 200 °C.

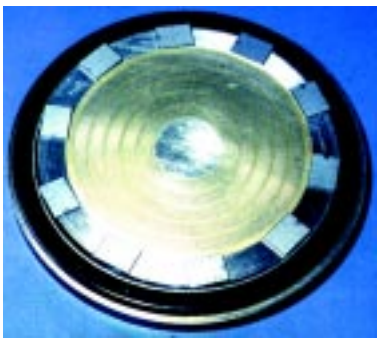


Fig. 5 - A photograph of a silicon MOS turn-off thyristor (MTO) showing a hybrid assembly of silicon gate turn-off thyristors (GTO) and silicon MOSFETs (photo courtesy of Silicon Power Corporation).

Low inductance, fast turn-off

Our approach to SiC power switching devices is based on a new device called the hybrid JFET Controlled Thyristor (JCT) (patent pending) shown in Fig. 6.

The advantages of the hybrid approach are

1. The high-power GTO and the low-power JFET can be independently optimized and separately processed.

2. The hybrid assembly may be operated at junction temperatures as high as 500 °C, resulting in reduced cooling requirements and reduced weight and volume.

In the case of JCT, the four-layer, *normally off* thyristor structure ($p^+np^-n^+$) (Fig. 7) is turned on in a conventional manner by injecting gate current of appropriate polarity through the GTO gate while keeping the JFET off (i.e., a negative voltage is applied to the JFET gate). This structure has been inverted from the conventional silicon structure due to the high resistance of the p^+ SiC substrates. The turn-on transition usually requires a small gate current, typically 1% to 2% of the anode current. The p^- blocking layer is used for forward blocking. However, unlike the GTO, where the structure is turned off by reversing the gate current on the GTO gate, the JCT is turned off by means of turning on the *n*-channel JFET (JFET gate is returned to 0 V). This shorts out the forward-biased p^+n junction, and the current is bypassed through the JFET (Fig. 6). This avoids complex gate drive snubbers currently employed to turn off silicon GTO devices due to very high gate currents involved. This *n*-channel JFET should have a breakdown voltage of about 25 V and current handling capability of about 30% to 50% of the rated GTO current, depending upon how fast one needs to turn the GTO off.

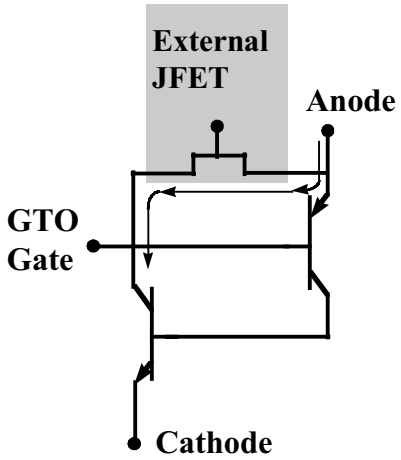


Fig. 6 - The JFET Controlled Thyristor (JCT) is an ideal power switching device in SiC. The proposed approach is based on the hybrid assembly using 4H-SiC GTO and 4H-SiC vertical JFETs. The hybrid JCT is turned off by diverting a sizable part of the main current through the external JFET.

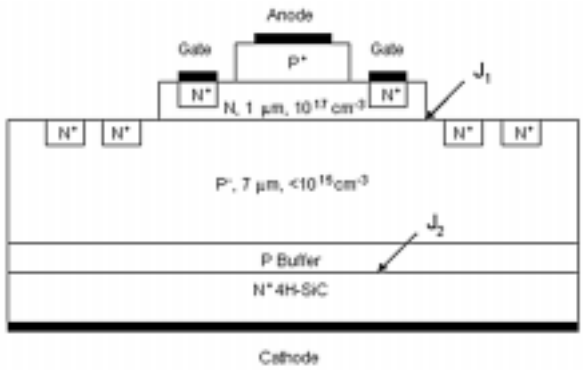


Fig. 7 - A schematic cross section of the SiC asymmetrical GTO cell. The thickness of the p^- base layer is adjusted for a given breakdown voltage.

Thermal Considerations

The performance of present-day silicon devices is limited by the thermal characteristics of devices and their packaging. Silicon devices are limited by the junction temperature limit of 150 °C (where typically a 125 °C temperature drop is experienced between the junction and the ambient). On the other hand, silicon carbide devices operating at 500 °C can more than quadruple the power density of power control modules. The removable heat flux can be increased by

450% simply by allowing the junction temperature to rise to 500 °C. Furthermore, significant reduction in the thermal impedance of the packaged parts is possible as thermal conductivity of SiC itself is three times better than Si at offering lateral heat spreading.

The performance of any power device is ultimately limited by the power dissipation within its structure, which determines the temperature rise:

$$\Delta T = T_J - T_A = P_D R_\theta$$

where P_D is the power dissipation, T_J is the junction temperature, T_A is the ambient temperature (25 °C), and R_θ is the thermal resistance. Typically, R_θ is dominated by the package and for an advanced, double-sided, passively cooled, bonded package aided by lateral spreading of heat in SiC, we can expect an R_θ of 0.15 °C/W. Assuming a junction temperature of 500 °C, we can dissipate about 3000 W/cm^2. If the device is operated at 500 A/cm^2 at 4 V forward drop, the conduction losses will be only about 2000 W/cm^2. Therefore, the switching frequency for a given application will be determined by the switching losses of the switch which, in turn, depend upon the turn-off time of the switch. A higher switching frequency is useful in reducing the size of the magnetic components in a typical power conversion system. A switching frequency of 50 to 100 kHz is desirable but generally not achievable in silicon devices.

Asymmetrical vs Symmetrical GTO

Figure 7 shows a schematic cross section of a 1-kV asymmetrical GTO cell [2,3]. The substrate is n^+ 4H-SiC doped with nitrogen to above 1×10^{19} cm^{-3}. The *p*-type layer consists of an ~1-μm p^+ buffer layer doped with Al to about 10^{18} cm^{-3} and a 7-μm p^- drift layer doped with Al at less than 1×10^{15} cm^{-3}. Next, there is a base layer of *n*-SiC, ~1 μm thick, doped with nitrogen at about 10^{18} cm^{-3}. Finally, the topmost layer is a very highly doped p^+ layer, doped with Al and about 0.7 μm thick. The width of the anode stripe is in the 15 to 50 μm range. The reverse blocking capability is minimal due to the presence of the p^+ buffer layer.

It turns out that the typical pulse width modulating (PWM) inverter systems need only asymmetrical switches. It is much easier to fabricate such devices because only one blocking junction (J_1) needs to be properly terminated. Our design uses floating n^+ guard rings to terminate this junction. This enables use of the multichip approach on the same SiC wafer because now small cells can be individually terminated. Symmetrical devices, however, will have two blocking junctions — J_1 and J_2 — one on each side of the drift layer, and no *p*-buffer layer. This means that symmetrical devices will have to be cut out of the wafer and beveled on the edges to achieve edge termination. This makes the multicell approach on the same host wafer almost impossible to implement as the cells tend to be small (~ 1 mm in diameter). In addition, it is much easier to grow the lightly doped, thick, *p*-type epitaxial layers required for asymmetrical devices than the precisely doped, half-as-thick *p*-type layers required for symmetrical devices.

Experimental Results

Figures 8 through 10 show the results on various devices. The "*involute*" structure has a diameter of 680 μm and carries a forward current of 4 A (J~1100 A/cm^2). The breakdown voltage of this device is 600 V.

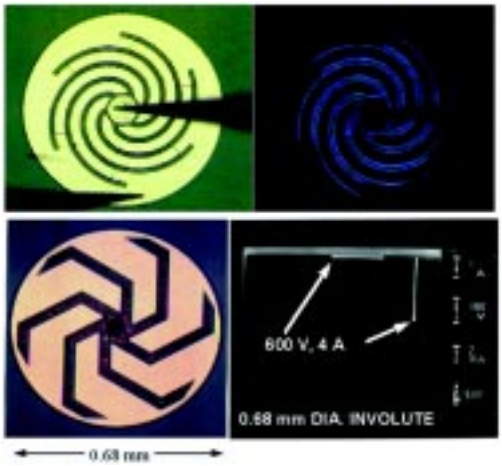


Fig. 8 - The "*involute*" design of SiC GTO shows 600 V forward blocking voltage and 4 A forward current at room temperature. The blue glow indicates that the device is fully turned on.

Figure 9 shows the forward current density vs forward drop of SiC GTO at different temperatures. The measurement was done with a gate current of 50 mA. The forward voltage drop is higher than expected due to poor contact resistance (~10^{-3} ohm • cm^2) of Ti/Al alloy to p^+ anode and the resistance of the bulk n^+ wafer (0.03 ohm • cm, 300 μm thick). The forward current density of 500 A/cm^2 is considered practical. Any higher value will result in excessive conduction losses. The forward drop reduces at elevated temperatures as expected. The turn-off transient was measured on six interdigitated devices in parallel (Fig. 10). The packaged device was turned off with a unit current gain from 3 A forward conduction. The measurements indicate a storage time of 130 ns and a fall time of 55 ns. These

results clearly demonstrate the potential for a higher switching speed up to 50 to 100 kHz. The scale-up strategy, shown in Fig. 11, entirely depends upon the expected improvements in the materials technology. For now, smaller cells can be connected in parallel to show large current handling capability. It is expected that within 2 to 3 years, the defect density in the material will reduce to below 1 cm^{-2}, thus enabling a 200 A single-cell-part.

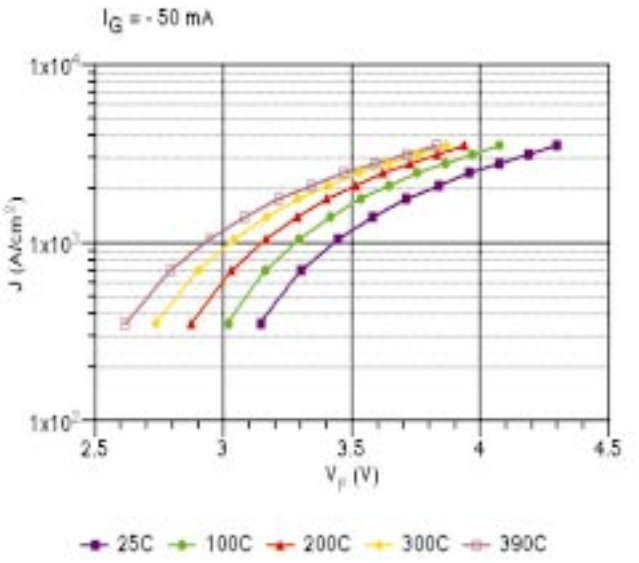


Fig. 9 - Forward current density vs forward drop of SiC GTO at different temperatures. The measurement was done with a gate current of 50 mA.

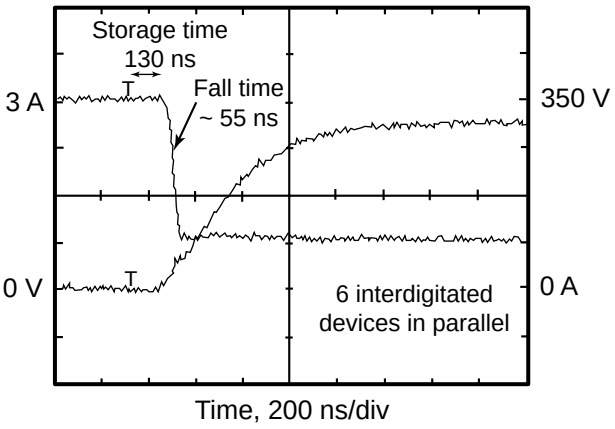


Fig. 10 - Turn-off transient measured on six interdigitated devices in parallel. The packaged device was turned off with a unit current gain from 3 A forward conduction. The results indicate a storage time of 130 ns and a fall time of 55 ns (courtesy of Silicon Power Corporation).

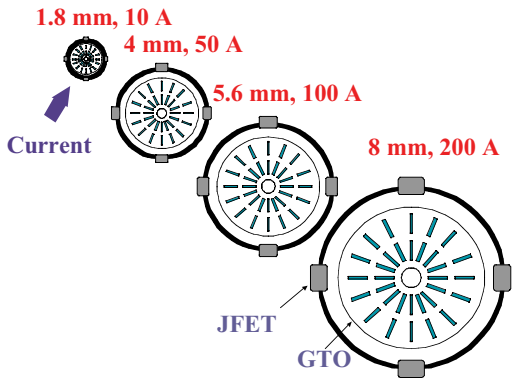


Fig. 11 - The GTO size projections with improvements in materials quality indicates that a 200-A part may be possible within 2 to 3 years. The current density has been assumed to be 500 A/cm^2.

Power MOSFET Devices

In the area of power switching devices, vertical power MOSFETs (Fig. 12) and IGBTs have been demonstrated [4-10], but with more limited success because of the high interface trap density (~5×10^{11} $cm^{-2} \cdot eV^{-1}$) and high fixed-oxide charge (~10^{12} cm^{-2}) for thermally grown gate oxides. We have fabricated vertical UMOSFETs on 4H-SiC with breakdown voltages up to between 1100 and 1400 V (Fig. 13).

Due to the smaller barrier heights for electron injection from the SiC conduction band into the silicon dioxide conduction band as compared to Si, the time dependent dielectric breakdown (TDDB) and hot electron injection are expected to be serious reliability issues. This is especially so if high temperature (greater than 200 °C) operation is considered [11]. This raises serious concerns about the

UMOSFET. MOSFET with U-shaped gates.

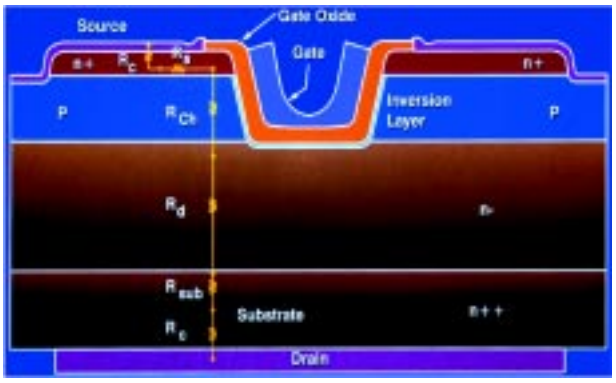


Fig. 12 - A schematic cross section of a unit cell of the SiC UMOSFET showing high field points under on or off conditions.

reliability of SiC power MOS devices operating at elevated temperatures. Long-term TDDB measurements are needed to determine a maximum limit on the electric field across the gate oxide in a 4H-SiC MOS system; however, it is clear that this maximum electric field should be much lower than that of silicon. It should be even lower for operation at higher junction temperatures. This would adversely impact the on-resistance of the inversion layer. Detailed Fowler-Nordheim measurements [11] indicate that at a given temperature and electric field, the current density in 4H-SiC MOS systems is about five times higher than that of 6H-SiC systems because of the 4H-SiC MOS system's smaller effective barrier height. These reliability concerns make the usefulness of power MOSFETs and IGBTs somewhat questionable for high temperature operation.

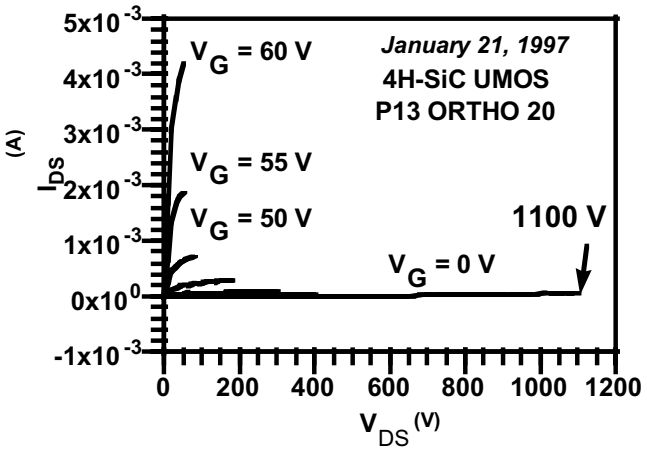


Fig. 13 - Experimental or I-V characteristics at 300 °C of a 4H-SiC UMOSFET indicating 1400 V breakdown voltage.

The SiC MOSFET devices have been found to have a very low inversion layer electron mobility (1 to 10 cm^2/Vs) as evidenced by the I-V curves of Fig.13. This has generally been attributed to high interface trap density near the conduction band edge. Recently, we have discovered that if ion-implanted regions are annealed above 1400 °C, the surface of the SiC gets very rough due to the phenomenon called "step-bunching." The rms value of this roughness can be a few hundred Å as shown in Fig. 14. This surface roughness is responsible for the poor inversion layer mobility of electrons in these devices. We have recently made lateral devices on 6H-SiC with inversion layer electron mobility of about 55 cm^2/Vs [12] by avoiding step-bunching, as shown in the I-V plots of Fig. 15.

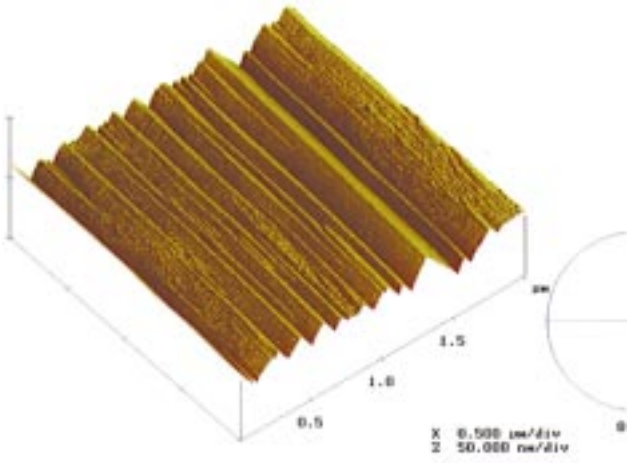


Fig. 14 - An atomic force microscopy (AFM) picture of a SiC surface annealed at 1600 °C showing rms roughness of about 100 Å.

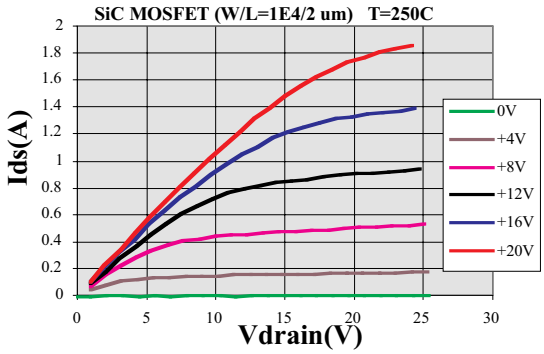


Fig. 15 - The I-V characteristics of lateral MOSFETs made on 6H-SiC. Oxide thickness ~340 Å, W/L = 1 cm/2 µm.

Conclusions

We have presented an overview of SiC power devices and concluded that the JFET Controlled Thyristor (JCT) is the most promising SiC switching device for high-power, high-temperature applications such as the All Electric Combat Vehicle due to its ease of turn-off, potential for 500 °C operation, and resulting reduction in cooling requirements. In order to take advantage of SiC power devices, high-temperature packages and components with double-sided contact need to be developed concurrently. Devices such as MOSFETs and IGBTs will be unreliable at high temperatures due to fundamental issues such as charge injection and trapping in the insulating layers. 6H-SiC is better in this respect because it offers a higher barrier height for electron

injection from conduction band into oxide and higher inversion layer electron mobility. The phenomenon of "step-bunching" explains the previously obtained low surface electron mobilities. Finally, for future scaling up of these devices, it is important to reduce not only micropipes but the dislocation density from the low current levels of 10^4 cm^{-2} by at least an order of magnitude as well.

Acknowledgments

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Suresh Seshadri received a B.S. degree in electrical engineering from Columbia University and a Ph.D. in electrical engineering from Yale University. His Ph.D. dissertation examined mechanisms for compositional disordering of AlGaAs quantum well heterostructures. In 1995, he became a senior engineer at Westinghouse Science & Technology Center (W-STC) where he was part of a group responsible for developing the first practical SiC neutron detectors for high radiation environments, an achievement for which the group received a 1997 Westinghouse Signature Award for Excellence. Continuing work on the development of SiC/GaN diodes for wideband RF amplification at W-STC after its sale to Northrop Grumman Corporation in 1997, he has since been primarily involved in the development of SiC diodes, Gate Turn-Off (GTO) and MOS Turn-Off (MTO) thyristors, and the Junction Controlled Thyristor (JCT) for high-temperature, high-frequency, and high-power switching applications. This work has recently culminated in the first demonstration of an all-SiC Pulse Width Modulated (PWM) inverter. He has authored/coauthored 22 publications.

Jeffrey B. Casady received his B.S.E.E. and his M.S.E.E. from the University of Missouri, Columbia, in 1990 and 1992, respectively, and his Ph.D. in electrical engineering from Auburn University in 1996. His Ph.D. dissertation was performed on advanced SiC unit process development and device characterization/implementation. After receiving his Ph.D., he worked for approximately 2-1/2 years at Northrop Grumman Corporation, Electronic Sensors & Systems Sector, as a senior engineer. While at Northrop Grumman, he researched advanced SiC power and microwave device design and processing. He designed and processed SiC GTOs, UMOSFETs, DMOSFETs, and SITs for a variety of externally and internally sponsored programs. He then joined Mississippi State University as an Assistant Professor of Electrical Engineering in January 1999 to continue his research into wide bandgap semiconductor devices. Over the past five years, principal publications include more than 35 technical articles relating to SiC devices, including one book chapter. In addition to his technical activities, Dr. Casady has been a member of IEEE for 11 years, and is a member of both the IEEE Electron Device Society and IEEE Power Electronics Society, as well as a member of Eta Kappa Nu. In 1997, he received a Northrop Grumman award for timely contributions in the development and fabrication of SiC UMOSFETs.

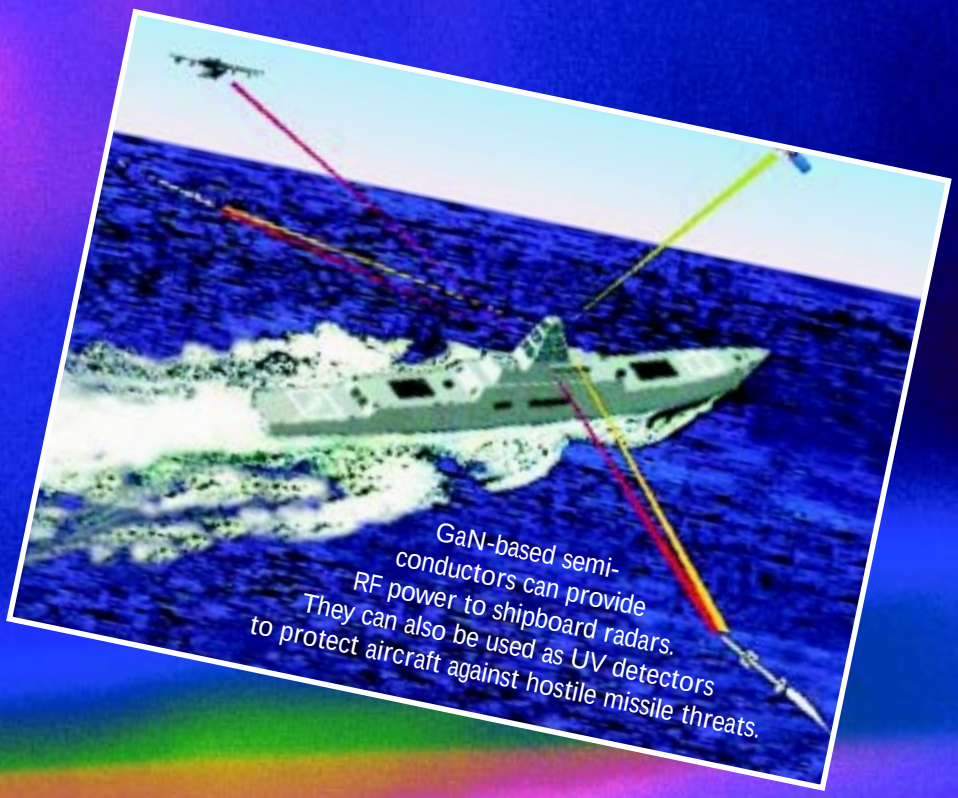
Phillip A. Sanger received his B.A. degree in physics from Saint Louis University in 1970. Following a Fulbright year of study in nuclear engineering at Saclay, France, he resumed his graduate studies at the University of Wisconsin, Madison, Wisconsin, where he received his M.S. in 1974 and, ultimately, his Ph.D. in 1977. He performed his thesis research at Fermilab in Batavia, Illinois, on the effects of 400 GeV protons on metals. From 1977 to 1989, he pursued the development of superconductors and superconducting MRI systems at Oxford Superconducting Technology, Carteret. Following a brief period with the Superconducting SuperCollider Laboratory in Dallas, Texas, between 1989 and 1992, he has been engaged in managing the development of new technologies at the Northrop Grumman Science and Technology Center in Pittsburgh, Pennsylvania. Since 1996 he has pursued SiC power devices for military and commercial power conditioning applications.

Charles D. Brandt has been working in the semiconductor field for the last 19 years in three primary areas of research: growth and characterization of GaAs and InP crystals, III-V integrated circuit fabrication, and wide bandgap (SiC, GaN) materials and device development. His early work on bulk crystals was directed at the behavior of the transition elements V, Ti, and Sc as dopants in GaAs, InP, and AlGaAs and involved the use of crystal growth techniques such as liquid-encapsulated Czochralski and horizontal Bridgman in addition to extensive electrical and optical characterization. As a staff member at Raytheon's Research Division in the early 1980s, he was involved in the formulation of plasma deposition and etching techniques suitable for GaAs FET fabrication. In recent years, Dr. Brandt's work at Northrop Grumman has centered around the development of advanced SiC-based devices covering the range from DC to Ka band, where he has managed development programs for SiC SITs, MESFETs, MOSFETs, IMPATTs, GTOs, and diodes. He has also been extensively involved in the development of advanced processing and packaging techniques for monolithic microwave integrated circuits utilizing wafer-scale integration concepts. Dr. Brandt has over 50 technical publications in these areas. Currently, Dr. Brandt manages the Microelectronics Department at the Northrop Grumman Science & Technology Center in Pittsburgh, Pennsylvania.

Nelson Saks received his B.A. degree in physics from Amherst College in 1968 and his M.S. degree in physics from the University of Maryland in 1973. He has held the position of research physicist at the Electronics Science and Technology Division of the Naval Research Laboratory, Washington, D.C., from 1968 to the present. He has worked on amorphous semiconductors, development of charge-coupled devices, and MOS devices with an emphasis on electrical characterization techniques and radiation effects. Mr. Saks has enjoyed sabbaticals at IMEC, Leuven, Belgium, where he worked on hot carrier injection in VLSI devices (1984-1985) and at Northrop Grumman Corporation, Pittsburgh, Pennsylvania, where he worked on SiC power devices. He has been active in the radiation effects community and was technical program chairman of the 1992 IEEE Nuclear and Space Radiation Effects Conference. He served as advisor to the Defense Nuclear Agency from 1988 to 1995 on the basic mechanisms of radiation damage in electronic devices. His present interests include hot carrier injection phenomena in MOSFETs; techniques for characterizing MOS devices, especially charge pumping; growth and characterization of MOS gate dielectrics; basic mechanisms of radiation damage in MOS structures; MOS devices on SiC and GaN; and lifetime in MOS power devices. He has authored or coauthored more than 100 publications on these topics. Mr. Saks was elected Fellow of the IEEE in January 1996 for "contributions to the understanding of the basic mechanisms of radiation damage in metal-oxide-semiconductor devices."

a "MODFET" is not a 1960s-style festival . . .

rather, it is a modulation-doped field effect transistor, a kind of metal-oxide semiconductor FET in which a thin layer of a nitride semiconductor is deposited on an undoped, and therefore electrically highly resistive, substrate. The alloy nitride confines the electrons to a quantum mechanical well that enhances their ability to move about in the plane, thus increasing the device performance. In MODFETs, GaN can go where no semiconductor has gone before, and is therefore in increasing demand in high power, high temperature applications. This is because of its large bandgap, high breakdown voltage, high thermal conductivity, and high electron velocities. Nitride semiconductors are also sought after for use in optoelectronic devices that operate in the UV and visible wavelengths. When used as UV sensors, GaN devices have shown tremendous promise in applications that range from maximizing fuel efficiency to detecting threats aimed at aircraft. In MODFETs,



GaN-based semiconductors can provide RF power to shipboard radars. They can also be used as UV detectors to protect aircraft against hostile missile threats.

GaN has demonstrated record power levels at high frequencies. The nitrides (GaN and its heterostructures with InGaN and AlGaN) used as light-emitting diodes (LEDs) and laser diodes (LDs) are already being applied to scores of applications as diverse as computers and traffic signals; they are excellent candidates for an even wider diversity of technologies that include printing, agriculture, and health care.

In this article, Dr. Hadis Morkoç of Virginia Commonwealth University, one of the most cited physicists in the world because of his groundbreaking research in many semiconductor composites, including wide bandgap semiconductors, delivers a state-of-the-art address on the latest research and development of GaN-based MODFETs and UV detectors. Besides exploring their promising potential, he explains the science behind how they do what they do.

– S.O.

A field effect transistor (FET) is built by molecular beam epitaxy (MBE) from two layers of semiconducting material. The top layer is active (current can flow), and the bottom layer is semi-insulating. The top layer is composed of a source (of electrons), a gate, and a drain. When voltage is applied to the gate, this material allows electrons to flow from the source to drain, thus amplifying voltage.

GaN-Based Modulation-Doped FETs and UV Detectors

Hadis Morkoç

Virginia Commonwealth University
Richmond, Virginia

Introduction

Semiconductor nitrides such as aluminum nitride (AlN), gallium nitride (GaN), and indium nitride (InN) are very promising materials for their potential use in optoelectronic devices (both emitters and detectors) and high power/temperature electronic devices as have been treated in length and reviewed recently [1-5]. These materials and their ternary and quaternary alloys cover an energy bandgap range of 1.9 to 6.2 eV, suitable for band-to-band light generation with colors ranging from red (potentially) to ultraviolet (UV) wavelengths. Specifically, nitrides are suitable for such applications as surface acoustic wave devices [6], UV detectors [7,8] Bragg reflectors [9], waveguides, UV and visible light emitting diodes (LEDs) [10-12], and laser diodes (LDs) [13] for digital data read-write applications. During the last several decades, lasers and LEDs have expanded remarkably both in terms of the range of emission wavelengths available and brightness. The nitride semiconductor-based LEDs have proven to be reliable in such applications as displays, lighting, indicator lights, advertisement, and traffic signs/signals; possible applications include use in agriculture as light sources for accelerated photosynthesis, and in health care for diagnosis and treatment. Lasers, as coherent sources, are crucial for high-density optical read and write technologies. Because the diffraction-limited optical storage density increases approximately quadratically as the probe laser wavelength is reduced, nitride-based coherent sources at wavelengths down to UV are attracting a good deal of attention. Optical storage would enable the storage and retrieval of inordinate numbers of images and vast quantities of text with untold efficiency. Other equally attractive applications envisioned include printing and surgery.

When used as UV sensors in jet engines, automobiles, and furnaces (boilers), the devices would allow optimal fuel efficiency and control of effluents for a cleaner environment. Moreover, UV sensors that operate in the solar blind region (260 to 290 nm) would have high detectivity because the ozone layer absorbs solar radiation at those wavelengths, thus virtually eliminating radiation noise. Consequently, these detectors are expected to play a pivotal role in threat recognition aimed against aircraft [7,8,14]. GaN/AlGaN UV *p-i-n* detectors have demonstrated sensitivities of about 0.12 A/W and response speed of a few nanoseconds in 250 μm dot sizes; both values represent a quantum leap over previous capability.

GaN's large bandgap, large dielectric breakdown field, fortuitously good electron transport properties, and good thermal conductivity are conducive for use in high power electronic devices [15]. Sheppard et al. [16] have already reported that 0.45 mm gate, high power modulation-doped FETs (MODFETs) on SiC substrates exhibited a record power density of 6.8 W/mm in a 125 μm-wide device and a record total power of 4 W (with a power density of 2 W/mm) at 10 GHz. Other groups have also reported on the superior performance of GaN-based MODFETs on SiC and sapphire substrates with respect to competing materials, particularly at X band and higher frequencies [17-19]. Applications include use in amplifiers operative at high temperature and in unfriendly environments as well as in low-cost compact amplifiers for earthbound and space applications.

Nitride semiconductors have been deposited by vapor phase epitaxy (i.e., both hydride VPE [HVPE] and organometallic VPE [OVPE]), and in a vacuum by molecular beam epitaxy (MBE). With its innate refined control of growth parameters, *in-situ* monitoring capability, and uniformity, MBE is well suited for depositing heterostructures and gaining insight to deposition/incorporation mechanisms. MBE's control over growth parameters is such that any structure can be grown in any sequence. The structures for IR lasers in CD players, surface emitting vertical cavity lasers, and high-performance electronic devices such as pseudomorphic MODFETs have all been produced very successfully, most

of them commercially, by MBE. Nitride growth, however, requires much higher temperatures than those used in producing the conventional Group III-V semiconductors for which the MBE systems were designed. In addition, it has proved difficult to provide active N species at sufficiently high rates for nitride growth. Despite these mechanical/engineering limitations and its relatively late entry, MBE has already played a key role on a number of fronts, such as high performance GaN-based MODFETs and fast solar blind detectors, which are discussed in this article.

Modulation-Doped Field Effect Transistors

With its reduced impurity scattering and unique gate capacitance-voltage characteristics, the MODFET has become the dominant high frequency device. Among the MODFET's most attractive attributes are close proximity of the mobile charge to the gate electrode and high drain efficiency. As in the case of emitters, the GaN-based MODFETs have quickly demonstrated record power levels at high frequencies.

In MODFETs, the carriers that form the channel in the smaller bandgap material are donated by the larger bandgap material, ohmic contacts, or both. Since the mobile carriers and their parent donors are spatially separated, short-range ion scattering is nearly eliminated, which leads to mobilities that are characteristic of nearly pure semiconductors. A Schottky barrier is then used to modulate the mobile charge that in turn causes a change in the drain current. Because of this heterolayer construction, the gate can be placed very close to the conducting channel, resulting in large transconductances [20]. Figure 1 presents a schematic representation of a GaN/AlGaN MODFET structure in which the carriers are provided by the donors in the wider bandgap AlGaN. In a MODFET device, the carriers can also be provided by the source contact.

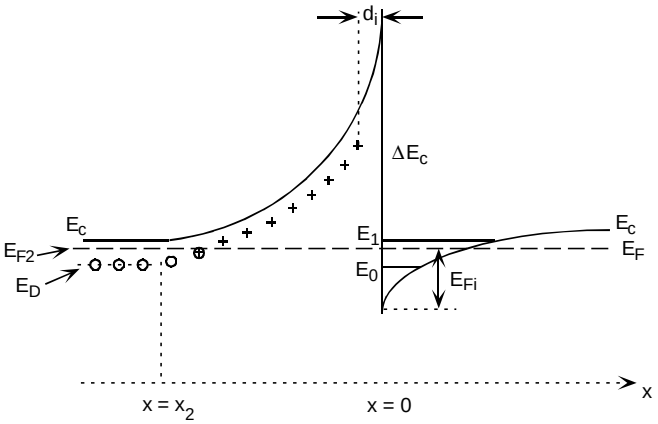


Fig. 1 - Conduction band structure of a modulation-doped structure.

Polarization

Polarization charge, however, affects device design and operation in all nitrides, particularly nitride-based MODFETs. Polarization charge arises from two sources: piezoelectric (PE) effects and the difference in spontaneous polarization between AlGaN and GaN, even in the absence of strain. Spontaneous polarization has only recently been fully understood. As shown in Ref. 21, nitrides lack inversion symmetry and exhibit piezoelectric effects when strained along the [0001] direction. Piezoelectric coefficients in nitrides are almost an order of magnitude larger than in traditional Group III-V semiconductors [22]. In addition, wurtzite GaN has a unique axis, thus allowing spontaneous polarization ($\mathbf{P_0}$, whose values are given in Table 1) even in the absence of strain. This can manifest itself as polarization charge at hetero-interfaces. Reference 23 provides a review of polarization effects.

WURTZITE. A three-dimensional hexagonal crystalline structure (such as the blade of a hex wrench).

Table 1 - Piezoelectric Constants and Spontaneous Polarization Charge in Nitride Semiconductors

	AlN	GaN	InN
e_{33}* [C/m^2**]	1.46	0.73	0.97
e_{31}* [C/m^2]	–0.60	–0.49	–0.57
$\mathbf{P_0}$ [C/m^2]	–0.081	–0.029	–0.032
[e_{31}-[c_{31}/c_{33}***]e_{33}]	–0.86	–0.68	–0.90

* e_{31} and e_{33} are piezoelectric constants
** C/m^2 is coulombs per square meter
*** c_{31} and c_{33} are elastic constants

Let us compare the relative importance of spontaneous polarization to piezoelectric polarization. For a biaxially strained layer, the effective piezoelectric polarization is given by

$$P_z^{piezo} = [e_{31}-(c_{31}/c_{33})e_{33}]\varepsilon_{\perp}, \qquad (1)$$

where $\varepsilon_{\perp} = \varepsilon_{xx} + \varepsilon_{yy}$ is the in-plane strain and c_{31} and c_{33} are elastic constants.

For $Al_xGa_{1-x}N$ pseudomorphically strained on a relaxed GaN substrate, the strain $\varepsilon_{\perp}$ is expected to be proportional to x and given by $\varepsilon_{\perp} = 2x(a_{GaN}-a_{AlGaN})/a_{AlGaN}$, which is $0.051x$ and is tensile. The piezoelectric polarization is then $P^{piezo} = -0.044x$, i.e., pointing in the [000$\bar{1}$] direction. The corresponding difference in spontaneous polarization between $Al_xGa_{1-x}N$ and GaN is also expected to be proportional to x and is given by $\Delta P^{spon} = -0.049x$. So, the two work in the same direction and are comparable in magni-

tude. Note that these are all in C/ m^2 and that $1C/m^2 = 0.624\times10^{15}$ electrons/cm^2. So, for *x* of order 0.1, we are dealing with carrier concentrations of order 10^{12}-10^{13}.

For an $In_xGa_{1-x}N$ layer, the situation is different: now, the difference in spontaneous polarization is much smaller, $\Delta P^{spon} = -0.003x$. Furthermore, the $In_xGa_{1-x}N$ layer on GaN would be under compressive stress $\varepsilon_{\perp} = -0.203x$, and $P^{piezo} = +0.183x$. Here the piezoelectric polarization dominates and is opposite in direction but even larger in absolute magnitude.

In the AlGaN case, the sign of the polarization is such as to produce a potential energy for electrons sloping down from the Ga face towards the N face. Thus, for a structure in which the Ga face is turned towards the surface, the potential will slope down from the AlGaN surface towards the AlGaN/GaN interface and helps to drive carriers towards the two-dimensional electron gas (2DEG) forming at this interface. For example, if there is an ohmic metal contact on the AlGaN surface, electrons will flow towards the 2DEG below that layer.

The most favorable situation for enhancing sheet carrier concentration would occur for an InGaN quantum well on top of relaxed *n*-GaN and below a AlGaN barrier with the whole structure having cation polarity towards the surface. In that case, the field will slope down towards the InGaN/AlGaN interface in the quantum well and will help localize the carriers in the 2DEG. Note that the piezoelectric polarizations estimated here are based on the theoretical values for a perfectly insulating material. The field is screened by the carriers present in each layer. For example, if carriers flow from a metal contact towards the 2DEG, then this will set up a counteracting field. The self-consistent field is ultimately determined by the condition that the chemical potential for electrons (i.e., the Fermi level) must be constant throughout the structure and thus depends on the doping and band bending in the substrate and, possibly, in each of the layers. At the least, one may expect these fields to be reduced by a factor corresponding to the macroscopic dielectric constant, i.e., a factor of order 10 but possibly larger if the layers acquire conductivity by free carriers. So, a more realistic expectation for the effects on sheet carrier concentration is of order 10^{11}-10^{12} electrons/cm^2.

The difference between these and traditional device structures without polarization effects is that for uniform dopant concentrations, one obtains parabolically varying potentials with distance, whereas here the linear terms come from polarization on top of the parabolic terms. These linear terms lead to variations of the potential over a shorter distance scale determined by the thickness of the layers, whereas the parabolic terms correspond to the space-charge regions. Thus the linear terms may help to localize carriers if the polarity of the structure is chosen properly.

Some further words of caution about the above estimates are needed. If the AlGaN layers are not pseudomorphic but partially relaxed (by misfit dislocations for example), then the piezoelectric effect would be reduced but the spontaneous polarization would still be present. If the interfaces are not atomically sharp but exhibit a certain degree of interdiffusion, the differences in spontaneous polarization would be reduced as well. Finally, if domains with inverted polarity exist, the overall polarization effects may be washed out. Also note that in an inverted structure with nitrogen (N) polarity towards the surface, it may be possible to create a two-dimensional hole gas (2DHG) at the AlGaN/substrateGaN interface, providing that free holes are available. However, if an *n*-type GaN layer is placed on top, a 2DEG may form on top of the AlGaN layer.

The immediate impact of this polarization is that the field generated by this process must be considered together with that induced by the applied voltage and charge redistribution. Moreover, as alluded to earlier, free carriers can also be drawn from any shallow and weakly bound impurities and metal in contact with the semiconductor. In any case, the free carriers would tend to screen the piezoelectric-induced polarization field. An additional complicating factor in nitrides in relation to polarization is that the semiconductor tends to twist and tilt in a columnar mode, in an effort to minimize strain as shown in Fig. 2. These columns do not have the same cation/anion ordering polarity as shown in Fig. 2. In the presence of strain, Ga polarity domains and N polarity domains would have opposite polarization, causing increased scattering [24-26].

Figure 3 is a schematic representation of an ideal inversion domain boundary formed in growth along the [0001] direction. On the left of the boundary, the growth initiates

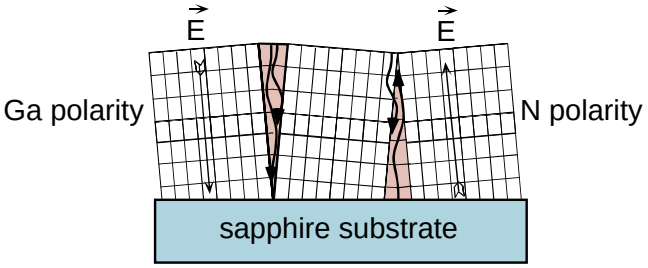


Fig. 2 - Domains in GaN, with N polarity (nitrogen surface layer) on the right and Ga polarity (with Ga on surface) on the left side under compressive residual strain. The arrows show the direction of the E field in each of the domains.

with N, and on the right it begins with Ga. On the left side, the bond along the [0001] direction is from Ga to N; this is called Ga polarity. On the right side, the [0001] bonds are from N to Ga; this is called N polarity. In N polarity and under tensile strain, the PE field generated points toward the surface, whereas that for the Ga polarity region points in from the surface. When the strain is compressive, the direction of the field changes.

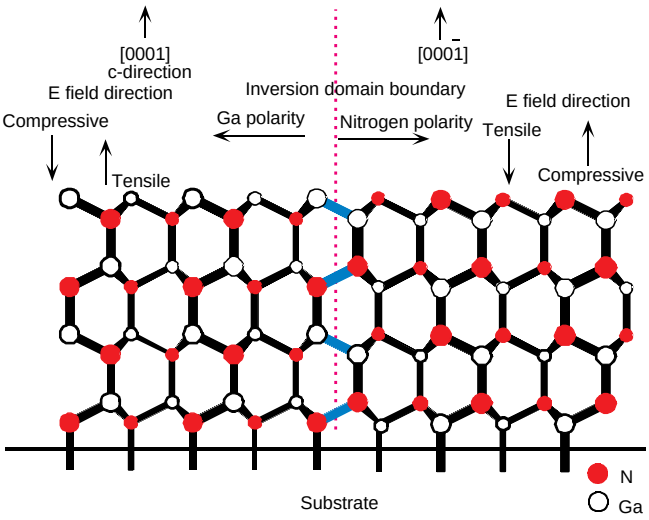


Fig. 3 - Schematic representation of an inversion domain boundary formed in growth along the [0001] direction.

Yet an additional complicating factor is the asymmetry in the barrier discontinuities between GaN and its binary and ternaries caused by spontaneous polarization [27]. The spontaneous polarization arises simply because of the ionicity of the bonds and the low symmetry in wurtzite. In fact, Bernardini et al. [28] showed that the field that occurs in quantum wells is almost completely determined by both the difference in spontaneous polarization between the two bulks, and their PE contribution. The field (i.e., the slope of the potential) is quite independent of the offset (i.e., the dipole discontinuity that occurs at the interface between the two materials). In other words, the dipole at the interface appears to be independent from the charge (monopole) accumulated at the interface. Recent experimental results obtained in the author's laboratory with colleagues from the University of Lecce support this theory in that the spontaneous polarization component is dominant.

MODFET Description

Simplified analytical descriptions of MODFET operation have been developed which show quantitatively the effect of charge stored at the hetero-interface on mobility and carrier velocity. The analytical model of Drummond et al. [29] describes MODFET operation well. The model provides analytical expressions that relate the channel charge to the gate and drain potentials and predict the current voltage characteristics. In short, the MODFET provides large mobile carrier concentrations in close proximity to the gate, which was previously unachievable. A similar model [15,30] has been developed for GaN/AlGaN MODFETs and used to predict their performance. In short, the favorable velocity field characteristics of GaN point to performance that is competitive with GaAs even in terms of small signal properties. In terms of power performance, GaAs devices are supplanted by GaN devices with increasing margin as the nitride technology evolves. There are, however, anomalies such as high- frequency current collapse/degradation that must first be understood and circumvented before the intrinsic properties of GaN can be fully exploited.

In addition to the small signal description, an accurate modeling of device power is very useful. In high power semiconductor devices, it is imperative that the effect of temperature on device performance is accounted for accurately. As in small signal modeling, the first step in power modeling is to establish the basic device geometrical factors that are needed to calculate the current voltage characteristics. Once these are known, the output characteristics superimposed with the load line can be used to estimate the power level that can be obtained from the device provided that it is not limited by the input drive as shown in Fig. 4. In Class A operation, the maximum power that can be expected from the drain circuit of a device is given by

$$P_{max} = \frac{I_{dson}\,(V_b - V_{knee})}{8} \qquad (2)$$

where I_{dson} is the maximum drain current (this is the drain current with a small positive voltage on the gate electrode), V_b is the drain breakdown voltage, and V_{knee} is the knee voltage as shown in Fig 4. The allowable positive gate voltage (≈ 1V) will depend on the channel doping and the work function of the gate metal. The positive gate voltage is limited by the onset of forward Schottky-diode current. The DC load line shown in Fig. 3 would be used in a Class A RF amplifier with the maximum drain voltage $V_d = V_b/2$. The slope of the load line is $1/R_L$ where R_L is the value of the load resistance at the output of the FET. What can be gleaned from Eq. (2) is that V_b and I_{dson} must be made as large as possible. The utility of wide bandgap semiconductors such as GaN in this juncture is that the drain breakdown voltage is larger than that in conventional Group III-V semiconductors. In general, the drain can be swung to

voltages up to within 80% of the drain breakdown for a 20% margin of safety. It should be pointed out that the maximum drain current in nitride semiconductor-based MODFETs is in the same ballpark as that of more conventional semiconductors. This implies that increased power handling capability is a direct result of large breakdown voltages and thermal conductivity and the fact that higher junction temperatures can be tolerated. Ability to increase drain bias increases the load resistance and makes it easier to impedance match, particularly in devices with large gate widths.

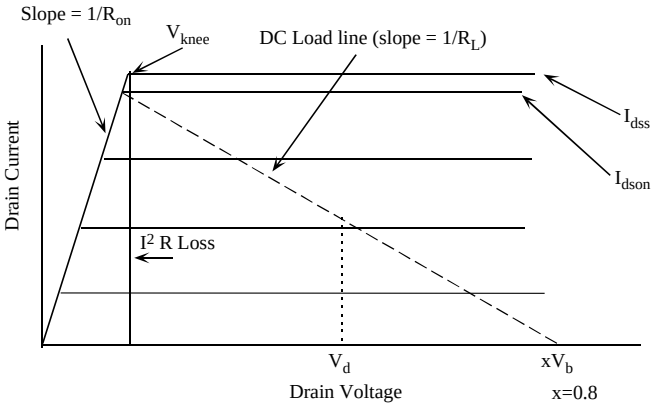


Fig. 4 - Pentode-like output I-V characteristics with the load line. The loss due to the on resistance is also indicated.

In power devices, power dissipation within the device increases the junction temperature and alters the output characteristics. On the one hand, higher junction temperatures with respect to the case temperature would enhance the heat dissipation to the power of four of the temperature differential, but along with it come reduced current and increased series resistances, which in turn increase the heat dissipation. Moreover, the thermal conductivity of the semiconductor decreases with increased temperature, exacerbating the situation. Consequently, the effect of junction temperature on the output characteristics must be taken into consideration. Temperature-dependent material parameters, if known, can be used to calculate the output characteristics with respect to temperature. However, a more pragmatic approach, particularly when the aforementioned parameters and or models required are not available, can be taken in which one measures the output characteristics of the device under consideration as a function of temperature. The junction temperature is critically dependent on the substrate thermal conductivity that is available for various substrates including GaN [1]. The functional dependence of thermal conductivity on temperature is

$$\chi(T) = \chi(T_0)\,(T/T_0)^{-r}, \qquad (3)$$

where the coefficient r is 0.559, 0.443, 0.524, and 0.544 for Si, GaAs, SiC, and sapphire, respectively [31]. Thermal conductivity of sapphire, SiC, GaAs, and Si as a function of temperature are shown in Fig. 5. In Fig. 5, $\chi(T_0)$ has also been appropriately reduced to account for the doping of the substrate material.

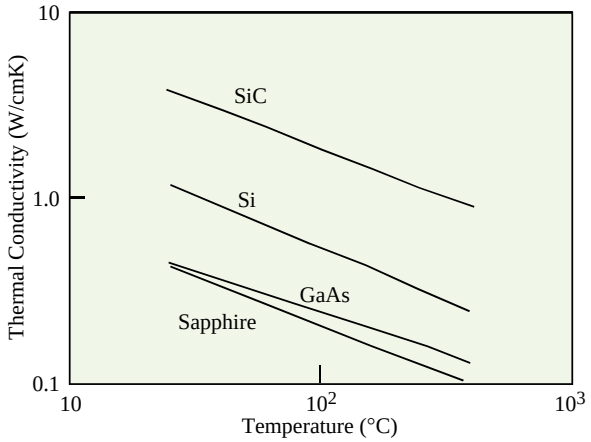


Fig. 5 - Thermal conductivity vs temperature for SiC and sapphire [31].

Schottky Barriers for Gates

Any semiconductor device requires metal contacts and MODFETs are no exception. These devices require ohmic source and drain contacts as well as a rectifying Schottky barrrier for controlling the charge in the channel. Schottky barrier-related processes for GaN-based devices are nascent, but rapid progress is being made. Until recently it has been difficult to fabricate good quality single-crystal films on which a Schottky metal could be deposited, and upon which the properties of Schottky barriers could be studied. However, considerable progress has been made with Pt-GaN Schottky barriers [32,33] that have been successfully implemented in GaN-based MODFETs [15,34-38].

Recent successes in growing good quality single-crystal Group III-V GaN layers prompted the fundamental electrical property studies of metal-semiconductor barriers on GaN. In order to determine the properties of only the metal-semiconductor junction, one must be able to model the semiconductor. Semiconductors with large defect concentrations are notorious for exhibiting parasitic processes in current-voltage and capacitance-voltage characteristics that cloud the picture. Consequently, good epitaxial layers as well as good metal-semiconductor interfaces are imperative. During the evolutionary period, while the sample quality is acceptable, temperature and frequency dependence of the capacitance-voltage characteristics and temperature-dependent current-voltage characteristics are measured and

analyzed for determining effective metal-semiconductor barrier height. To get a large Schottky barrier height for rectifying metal contacts on GaN, which is imperative for low leakage, metals with large work functions such as Au [39] and Pt [32] have been explored. Hacke et al. [39] have studied Schottky barriers made of Au on unintentionally doped *n*-GaN grown by HVPE. The forward current ideality factor was n_{idl} ~1.03 and the reverse bias leakage current was $<10^{-10}$ A at a reverse bias of -10 V. While the current-voltage measurement indicated the barrier height to be 0.844 eV, the capacitance measurements led to a value of 0.94 eV.

Suzue et al. [32] have studied the Pt Schottky barriers on unintentionally doped *n*-GaN. Temperature- dependent current-voltage and capacitance-voltage characteristics in the range of -195 °C to 42 °C were studied to gain insight about the current conduction mechanism. Any excess current observed is traditionally attributed to defects (generation recombination centers) and surface leakage current. The ensuing current is called the Shockley-Read-Hall (SRH) recombination current resulting from the mid-gap states. If one neglects this excess current, a barrier height of about 0.8 eV is deduced as opposed to about 1 eV deduced from the CV measurements. Because of the effect of excess current on the slope of the I-V curve, C-V measurements in this particular case may represent the metal barrier height. An examination of the C-V plots, however, indicated that under reverse bias condition, the capacitance depended insignificantly on the density of traps. The curves corresponding to all temperatures were largely linear, which yielded barrier heights ranging between 0.95 and 1.05 eV. Reduced capacitance with decreasing temperature is consistent with relatively deep donors. Binari et al. [40] determined Ti Schottky barriers heights to be 0.58 and 0.59 eV from the current-voltage and capacitance measurements, respectively. The ideality factor n_{idl} is approximately 1.28. The diode series resistance (R_s) is 100 W.

The ternary $Al_xGa_{1-x}N$ is an essential component of nitride-based MODFETs, which makes the investigation of metal $Al_xGa_{1-x}N$ contacts imperative. M. A. Khan et al. [41] reported the fabrication of a Cr/Au Schottky barrier on *n*-AlGaN. Moreover, M.R.H. Khan et al. [42] studied the Schottky barrier characteristics of the Au-$Al_xGa_{1-x}N$ system. A typical current-voltage characteristic of an $Al_{0.14}Ga_{0.86}N$ Schottky diode had an ideality factor of 1.56 under reverse bias and a threshold voltage of about 0.9 V at 0.1 A. The reverse bias leakage current was recorded to be marginally low (10^{-10} A) for a reverse bias of -10 V. By using the current-voltage method, the barrier height and electron affinity were determined to be 0.94 eV and 4.16 eV, respectively. From the C^{-2} vs V plot, the same barrier height and the electron affinity were deduced to be 1.3 ± 0.05 eV and 3.8 eV, respectively. As the AlGaN quality increases, periodic as well as more in-depth investigations will become necessary to get an accurate picture of intrinsic parameters. In short, the current conduction mechanism in metal-semiconductor structures is strongly affected by surface and bulk states. Deviations from an ideal ideality factor, such as is the case here, indicate such states. The situation gets more complicated with AlGaN and gets worse as the AlN mole fraction is increased. Likewise, capacitance-voltage measurements also are affected by states that are charged, either by interface state or by bulk state. As is the case in many facets of research and development, insights into the metal-nitride contacts will be gained in an evolutionary manner hinging upon the developments in nitride layers.

Contacts to GaN

Ohmic contacts in power devices are extremely important because they affect their efficiency as well as heat dissipation. Initial inferior results helped fuel concerns that GaN-based electronic devices may not perform well. Early specific contact resistivities on *n*-type GaN using Al and Au metallizations [43] were in the range of 10^{-4} and $l0^{-3}$ Ω cm^2. Major improvements were realized by using Ti/Au [44] and TiAl [45], in that specific contact resistivities in the high 10^{-6} Ω cm^2 were obtained with the latter. Carrying the TiAl contact work one step further, Wu et al. [46] confirmed that, except at very high annealing temperatures, the ohmic contact suggested by Lin et al. [45] functions very effectively. At very high temperatures, Al of the metal contact melts and tends to ball up, resulting in rough surfaces and increased ohmic contact resistances as pointed out already by Lin et al. [45]. In an attempt to circumvent this difficulty, Wu et al. [46] designed a separate layer-metallization method where a realignment and deposition of a second thin Ti layer, and a 2000 Å Au overlayer were carried out. Specific contact resistivities were in the range of 3.0×10^{-6} Ω cm^2 and 5.5×10^{-6} Ω cm^2, depending on the doping concentration in the semiconductor.

In an attempt to obtain improved ohmic contacts, Fan et al. [47] have designed a multilayer ohmic contact method. By using a composite metal layer of Ti/Al/Ni/Au (150Å/2200Å/400Å/500Å), they obtained very low contact resistivities. Specifically, for *n*-GaN with doping levels between 2×10^{17} cm^{-3} and 4×10^{17} cm^{-3}, they obtained specific contact resistivities in the range of ρ_s=1.19×10^{-7} Ω cm^2 and 8.9×10^{-8} W cm^2, respectively. Calculation of the contact resistivity was based on the assumption that the semiconductor sheet resistance underneath the contacts remains un-

changed, which is not true for nonalloyed contacts. As for the current conduction mechanism in these ohmic contacts, the large metal-semiconductor barriers diminish the possibility of thermionic-emission-governed ohmic contacts to GaN. The alternative mechanism is some form of tunneling that may take place if GaN is so heavily doped as to cause a very thin depletion region. Tunneling is possible if, due to annealing (for example, at 900 °C for 30 s), Al and Ti along with Ni undergo substantial interaction with each other and GaN. Investigations showed that Ti receives N from GaN, forming a metallic layer, while the lack of N on GaN provides the desired benefit of increased electron concentration through N vacancy formation [48]. Aluminum passivates the surface and also possibly reacts with Ti to form TiAl. Reference 2 provides further details.

AlGaN/GaN MODFETs

To reiterate, MODFET's performance is due to the conduction channel that allows large sheet carrier concentrations to be maintained and its unique capacitance-voltage relationship [49,50]. Moreover, spatial separation of scattering centers (such as ionized donors) from the electrons leads to low field transport void of ionized impurity scattering. What is somewhat unique to GaN and its alloys is its spontaneous polarization and the strain-induced piezoelectric effect [21,22,27,51-53] that causes redistribution of mobile and weakly bound charge and charge collected from metal contacts.

Stengel et al. [30] have recently modeled electronic properties of modulation-doped structures based on the III-nitride semiconductor system. The structure considered was a wurtzitic $Al_xGa_{1-x}N$/GaN normal MODFET. Because of the conduction band discontinuity, the electrons diffusing from the larger bandgap AlGaN into the smaller bandgap GaN form a triangular quantum well at the $Al_xGa_{1-x}N$/GaN interface, which is the hallmark of MODFETs. The source and drain contacts were assumed to penetrate down to the GaN layer that hosts the 2DEG.

To illustrate this, Fig. 6 shows the energy band diagram for a normally on (N-ON) MODFET calculated by Stengel et al. [30] for an AlN mole fraction of $x = 0.25$, a donor concentration in AlGaN, $N_d = 10^{19}$ cm^{-3}, and an undoped AlGaN layer thickness (spacer layer), $W_{sp} = 20$ Å. Also shown is the electron gas concentration at the heterointerface. For the simulated N-ON MODFET, a gate bias of $V_G = 0.04$ V, and doped AlGaN layer thickness of $d = 200$ Å were used. The 2DEG does not extend to the AlGaN region because of a high $Al_xGa_{1-x}N$/GaN conduction band discontinuity (more than 500 meV as compared to 142 meV for $Al_xGa_{1-x}As$/GaAs at $x = 0.3$). Because of this, and the fact that the probability of electron wave functions extending to the $Al_xGa_{1-x}N$ is very low, a thinner spacer would be sufficient to achieve the optimal mobility in the 2DEG due to a lower alloy scattering [54]. For the MODFET shown in Fig. 6, the quasi-Fermi level in GaN is far above the lowest energy level, and the peak volume concentration of electrons in the 2DEG is 10^{19} cm^{-3}. Also, some of the donor atoms (for z between -100 Å and -50 Å) are now neutralized, and some electrons start to appear in the $Al_xGa_{1-x}N$ region. Because of these, a further rise of the gate bias causes not only an increase in the donor neutralization, but also an increase in the electron concentration in $Al_xGa_{1-x}N$. However, the 2DEG concentration remains unaltered.

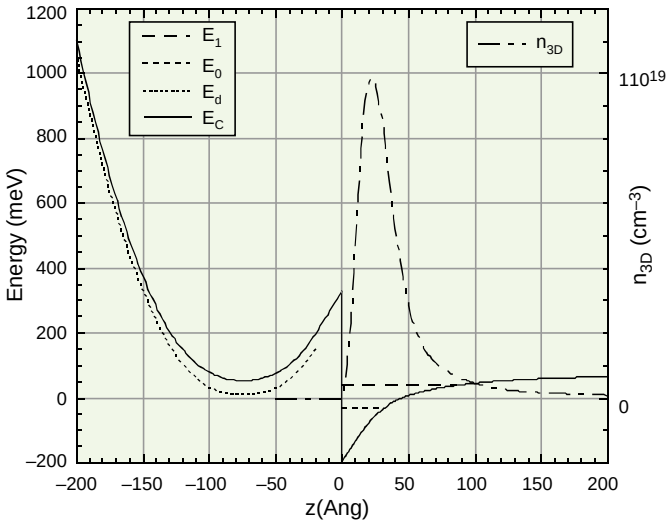


Fig. 6 - Band diagram for a normally on MODFET. The origin of energy for these band diagrams is the Fermi level. The left side of the $z = 0$ line corresponds to the AlGaN region and the right side to the GaN. The donor level in AlGaN is represented by E_d, and the quantum energy levels in GaN are represented by E_0 and E_1. The term E_c represents the conduction band edge in AlGaN and GaN layers.

Calculations employing typical parameters [30] for GaN and AlGaN indicate that the peak value of 2DEG concentration for $Al_xGa_{1-x}N$ /GaN MODFETs is around $2\text{-}5 \times 10^{12}$ cm^{-2}. However, much larger values of n_{2D} have been measured, which is most likely due to further ionization and redistribution of shallow charge by the piezoelectric effect that may also call for charge collection from metal contacts. Neglecting the piezoelectric effect, Fig. 7 shows n_{2D} vs V_G plots for various spacer thicknesses. As long as the unintentional doping level in the spacer layer is low, the effects of varying the AlN mole fraction, x, and W_{sp} on n_{2D} are essentially equivalent, because at the end of the spacer layer, the value of E_c-E_F is very close to E_c(interface)-W_{sp} (dE_c/dz) (inter-

face). Experimental data describing the effect of the spacer layer thickness on the mobility of electrons in the 2DEG are needed in order to evaluate optimized values for this spacer layer. However, one may predict that these values for the $Al_xGa_{1-x}N$ /GaN system would be smaller than those for the $Al_xGa_{1-x}As$/GaAs system, because the $Al_xGa_{1-x}N$ /GaN system provides a deeper confinement.

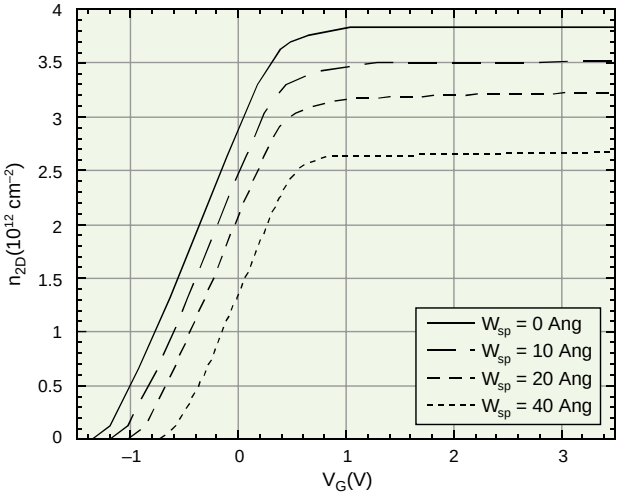


Fig. 7 - Plots of the 2DEG concentration as a function of the gate-source bias V_G for various values of the spacer layer thickness in $Al_xGa_{1-x}N$.

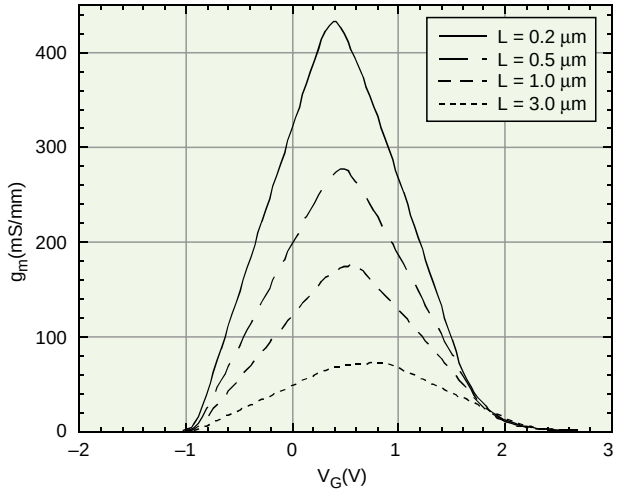


Fig. 8 - Variation of the transconductance g_m of MODFETs as a function of the gate-source bias V_G, at the optimal value of the drain-source bias V_D. The optimum value of V_D is defined to be the value at which the transconductance peak reaches its maximum value. The parameter is the channel length, L, with values of 0.2, 0.5, 1, and 3 mm. The parameters used for the 2DEG are d = 130 Å, $N_d = 10^{19}$ cm^{-3}, W_{sp} = 20 Å, x = 0.25, and E_d = 45 meV.

Stengel et al. [30] calculated the variation of transconductance with gate bias for various channel lengths as shown in Fig. 8. When the channel length was decreased from 1 to 0.2 mm, the peak transconductance increased from 420 to above 900 mS/mm. These very large transconductance values are much higher than those experimentally observed. They should change with improvements in layer quality and are made possible when the values of both V_G and V_D are chosen to be small to avert the velocity saturation of the carriers. This is indeed very encouraging considering that, for all practical purposes, MODFETs with reduced channel lengths are very desirable and have lower leakage currents at the operating point. Notably, the peak transconductance of these MODFETs is obtained for lower gate biases.

Experimental Performance of GaN MODFETs

Initial GaN MODFETs utilized the background donors in the AlGaN layer, the density of which is not controllable, to say the least, and any other free and weakly bound electrons drawn to the interface. Congruent with the early stages of development and the defect-laden nature of the early GaN and AlGaN layers, the MODFETs exhibited very low transconductances and a low-resistance and a high-resistance state before and after the application of a high drain voltage (20 V). As in the case of GaAs/AlGaAs MODFETs, hot electron trapping in the larger bandgap material at the drain side of the gate is primarily responsible for the current collapse. The negative electron charge accumulated because of this trapping causes a significant depletion of the channel layer, more probably a pinch-off, leading to a drastic reduction of the channel conductance and the decrease of the drain current. This continues to be effective until the drain-source bias is substantially increased, leading to a space-charge injection and giving rise to an increased drain-source current.

With improvements in the materials quality available, the transconductance, current capacity, and drain breakdown voltage are all increased to the point that GaN-based MODFETs are now strong contenders in the arena of high power devices/amplifiers, particularly at X band and higher frequencies. As is the case for FET device structure, improved and high resistivity buffer layers have once again played a pivotal role. For chronological purposes, a brief review of the latest class of MODFETs with high transconductances and current levels is given later in this article.

MODFETs with a gate length of 2 µm, gate width of 40 µm, and the drain-source separation of 4 µm exhibited drain currents of approximately 500 mA/mm and extrinsic

transconductances of approximately g_{em} = 185 mS/mm. The drain breakdown voltage for 1 μm gate to drain spacing was approximately 100 V, the exact value depending on the layer design and quality of the layered structure. Although terms such as piezoelectric doping are being used rather liberally to increase the sheet carrier concentration, ultimately regardless of the source of the carriers, the strength of the electric field that can be tolerated under the gate without excessive leakage will set an upper limit on the number of carriers that can accumulate at the interface and be modulated. Use of multi-2DEG structures is one obvious method to increase the current capability of MODFETs, and they have been employed. In those cases, the GaN layer is straddled by two doped AlGaN molecules that donate electrons to the channel, thus increasing the number of electrons available for current conduction. By Hall effect measurement, the mobility and sheet carrier densities in the 2DEG were about 304 cm^2/Vs and 3.7×10^{13} cm^{-2}, respectively, at room temperature. The sheet carrier concentration may have been affected by piezoelectric effect. A number of double heterochannel MODFETs (DHCMODFETs) with gate lengths of 1.5 to 1.75 μm and a gate width of 40 μm have been reported.

The maximum drain saturation current I_{DS} corresponding to a drain-source voltage V_{DS} = 7 V, and gate source voltage V_{GS} = 3.5 V in a DHCMODFET is about 1100 mA/mm, which is important because in high power devices, the input is momentarily forward biased. The DHCMODFET has a room temperature extrinsic transconductance of g_m = 270 mS/mm. The value of the total resistance R_T extracted from the linear region of the I-V curves is 4 Ω/mm. Near pinch-off, the drain breakdown voltage is about 80 V, indicating excellent power potential of the device. These measurements were made in a nitrogen- pressurized container to avoid possible oxidation of the contacts and probes. The maximum drain-source current and extrinsic transconductance of the DHCMODFET are 500 mA/mm and 120 mS/mm, respectively. These devices maintain reasonable output characteristics at temperatures as high as 500 °C with maximum drain current and extrinsic transconductance values of 380 mA/mm and 70 mS/mm, respectively. Cooling to room temperature restored the characteristics, which demonstrates the robustness of this material system and of the metallization employed. It should be noted, however, that high power operation requires large drain breakdown voltages with the added benefit of having large output resistances, which ameliorates impedance matching.

MODFETs have progressed to a point where microwave measurements have been performed on a variety of devices with gate lengths as wide as 2 μm and as narrow as about 0.2 μm. A typical MODFET structure with 2 μm gate lengths has been tested for small-signal S-parameters performed at bias conditions used for the power measurements (i.e., 15 V, -2.5 V, and 20 mA for the drain voltage, gate voltage, and drain current, respectively). The unity current gain cutoff frequency (f_t) and maximum frequency of oscillation (f_{max}) were 6 GHz and 11 GHz, respectively, at both 15 and 30 V bias. Values of f_t and f_{max} in excess of 50 GHz and 100 GHz have been reported for short channel (about 0.2 μm) devices, respectively. The power measurements for 2 μm devices were taken at 4 GHz with the input power swept from 5 dBm to 18 dBm in 14 steps. The input and output matches, which were used during the power sweep, were determined by iterating between source and load pulls. The output match was selected to optimize the output power, and the input match was selected to maximize the delivered power. The devices were biased to V_{DS} = 15 V and V_{GS} = -2.5 V. The I_{DS} at this bias was approximately 20 mA, which corresponds to 260 mA/mm. Devices exhibited 6 dB gain for various input levels. The maximum output power was 20.6 dBm, and the peak power added efficiency (PAE) was 17.5%. This corresponds to a normalized output power density of 1.5 W/mm. In general, devices on sapphire substrates suffer from the low thermal conductivity of sapphire substrates and exhibit negative differential resistance in the output characteristics. Remedies include better heat sinking by flip-chip mounting and the use of high resistivity 4H-SiC substrates, which provide good thermal conductivity but are hard to obtain.

GaN MODFET devices that have been grown in the author's laboratory on conducting 6H-SiC substrates exhibited output characteristics that lacked the negative resistance (i.e., they exhibited good heat sinking). There have subsequently been a few reports of MODFET power devices on high resistivity SiC [16,19,55] and *p*-type SiC [18] substrates with phenomenal improvement in power handling capability notwithstanding the rapid progress on sapphire substrates. On sapphire, recent 0.7-μm gate-length $Al_{0.5}Ga_{0.5}N$/ GaN MODFETs exhibited a current density of 1 A/mm, three-terminal breakdown voltages up to 200 V, and CW power densities of 2.84 and 2.57 W/mm at 8 and 10 GHz, respectively, representing a marked performance improvement for GaN-based FETs.

Unprecedented power levels are being achieved with near-half-micron gate lengths. With 0.7-μm gate length devices on SiC substrates, where the gate-source spacing and gate-drain spacing were 0.5 and 0.8 μm, respectively, a total output power of 2.3 W in a device with a 1.28 mm gate periphery has been obtained [19]. The power gain at the 2.3 W output power point was 3.6 dB with a PAE of 13.3%.

The power measurement was conducted at a drain voltage of 33 V. The current and power gain cutoff frequencies were 15 and 42 GHz. The contact resistance, though not the best, was between 2.6 and 3.5 Ωmm. The maximum normalized trans-conductance was 270 mS/mm, and the drain current was 293 mA/mm.

In power devices, the thermal limitation can never be eliminated completely as is the case in nitride devices, particularly when fabricated on sapphire substrates with a thermal conductivity of only approximately 0.3 W/cmK. Inclusion of thermal limitation leads to the results shown in Fig. 9 for devices that compete in the high-power device arena [15,31]. Since new device developments do in general compete with existing and alternative technologies, a brief account of competing technologies for power arena is given below. The Si metal semiconductor FET (MESFET) analytical curve, modeled for its simplicity, is slightly above the SiC analytical curve and indicates a maximum power density of 0.35 W/mm at V_{dS} = 7V, which is slightly lower than 0.39 W/mm. Since Si RF MESFETs are unavailable, commercial Si RF metal-oxide semiconductor FET (MOSFET) results were used for comparison instead. At low voltages, the Si MOSFET data parallel the analytical curve suggesting the validity of the functional dependence of power density on drain voltage. Also shown are two higher power density data points 0.4 W/mm, V_{dS} = 28V and 0.87 W/mm, V_{dS} = 48 V. These higher power densities were obtained with specially designed RF power MOSFETs that incorporate a lightly doped drain and field plates that significantly increase the breakdown voltage.

The GaAs analytical curve shows the highest power density of all of the devices at the lowest voltages primarily because

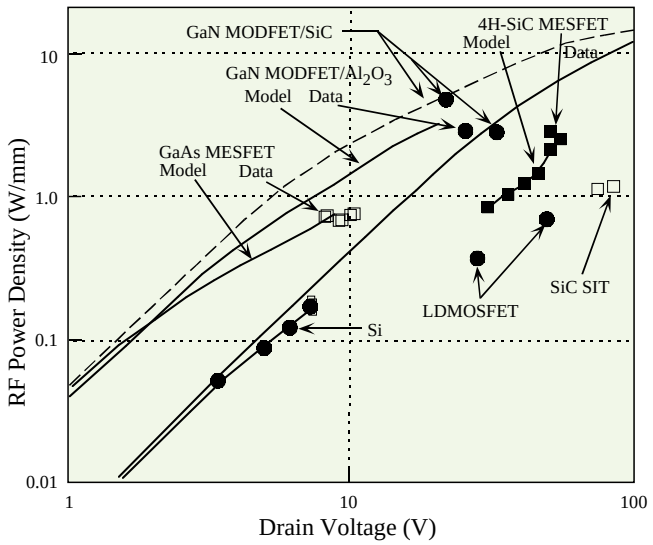


Fig. 9 - Simulated and experimental RF power density data for Si, GaAs, SiC, and GaN FETs [31].

of the higher electron mobility of GaAs. However, the low breakdown field limits the GaAs MESFET's drain voltage to about 8 V and power density to 0.63 W/mm including thermal effects. Typical commercially available GaAs MESFET power densities are below 1 W/mm. However, high-performance GaAs FETs with more complex device cross sections have achieved power densities as high as 1.4 W/mm at 18 V. At 100 V, the SiC MESFET has calculated maximum power densities of 7.96 W/mm with thermal effects and 9.7 W/mm without thermal effects. The highest demonstrated CW power density 3.3 W/mm (V_{ds} = 50 V) for a SiC MESFET [56] is also shown for comparison. Additional SiC data again illustrate the functional dependence of power density on drain voltage. The GaN analytical results are highly dependent on the thermal conductivity of the substrate. With a sapphire substrate, the device is severely thermally limited to 2.24 W/mm at 30 V with a resulting channel temperature of over 400 °C. With a SiC substrate, however, the analysis predicts that a GaN MODFET could achieve 15.5 W/mm at 100 V with a channel temperature of about 300 °C. To date, the highest power density achieved for a 0.45 μm × 125 μm GaN MODFET is 6.8 W/mm at 10 GHz with a PAE of 52.4% and an associated gain of 10.65 dB. At 16 GHz, the same figures in the same order are 4.4 W/mm, 27.3%, and 6.9 dB [16]. We should caution that while the power density figure can be used during the evolution process, eventually the total power figure must prevail. Normalized power density measurements, though frequently reported (a trap the present author also fell into), are often misleading because smaller gate widths naturally lead to larger power densities [16]. This experimental datum point is actually slightly higher than the simulated result, possibly because of the very small size of the experimental device (100 μm width).

The GaN results of analytical models are highly dependent on the thermal conductivity of the substrate. With a sapphire substrate, the device is severely thermally limited to 2.24 W/mm at 30 V with a resulting channel temperature over 400 °C. However with a SiC substrate, the analysis predicts that a GaN MODFET could achieve 15.5 W/mm at 100 V while keeping the channel temperature at about 300 °C [31]. The key to further improvements lies with our ability to control the polarity of the films, to prepare domain free material, and to reduce defects. If the past few years are any indication, substantial progress is in the wings.

Ultraviolet Detectors

The alloy AlGaN with about 50-60 % AlN absorbs in the region of the spectrum where the Sun's radiation is absorbed by the Earth's ozone layer, thereby providing a dark background. A detector operating in this region sees a dark

background that results in reduced radiation noise and allows the detection of minute emission from certain threats. UV (solar blind) detectors are imperative for the military in that they will enable airborne, sea borne, and ground equipment to detect and warn against ground-to-air, air-to-air, air-to-ground, and ground-to-ground missile threats. The system, at the heart of which is a UV detector, must be able to detect and track extremely weak signals from rapidly moving threats, which necessitates operation in the solar-blind region of the spectrum, 260 to 290 nm.

The continuing proliferation and increasing lethality of surface-to-air and air-to-air missiles pose serious threats to Air Force aircraft. Countering these threats successfully requires early detection of the missile launch. One promising method of detecting incoming missiles is sensing the UV emissions from the rocket plume. Particularly at altitudes lower than 20,000 ft, the solar-blind region is ideal for this purpose because the solar background radiation is almost entirely absorbed by atmospheric ozone. Thus, the ~3000 K blackbody emission from a missile plume stands out prominently against a dark background, thereby making false alarm rates very low.

Such a missile threat warning system, therefore, requires two-dimensional arrays of highly sensitive photodetectors to image the solar-blind UV spectral range. The current solution to this problem uses photomultiplier-type detectors and optical filters to block out all light except that between 260 and 290 nm. The problems with this approach are the limited sensitivity due to low transmission through the filters and low quantum efficiency of the photocathodes; the detection of wavelengths outside the solar-blind region caused by filter roll-off at wavelengths longer than 290 nm; and the large size and weight of the photomultiplier assembly and associated high-voltage power supply. By comparison, solid state detectors offer the advantages of being compact and rugged, of having near-unity quantum efficiency, and of having better rejection of long wavelength radiation due to their sharp UV band edge. Currently, however, no solid state UV photodetectors have the sensitivity required for this application.

Numerous papers concerning GaN and $Al_xGa_{1-x}N$ UV detectors have appeared in the literature. The detector structures reported include photoconductors (PCs), metal semiconductor-metals (MSMs), and photovoltaics (PVs, including Schottkys, *p-n* junctions, and *p-i-n*s). These detector structures were typically grown on sapphire substrates by variations of MBE and metal-organic chemical vapor deposition (MOCVD). Improvements in III-nitride materials growth and detector processing have resulted in progressively higher responsivity PV and PC ultraviolet detectors in the last few years [7,8,57-63]. In the past two years, $Al_xGa_{1-x}N$/GaN-based detector response times have decreased dramatically from the ms to the ns regime.

Ultraviolet detectors of the PV [8,61] and PC [58,64] varieties and based on nitride semiconductors prepared by MBE have been reported. Ultraviolet detectors fabricated in all MBE-grown materials have shown good quantum efficiencies, noise equivalent power, and speed of response. We only make brief mention of photoconducting detectors in this article because they suffer from large dark-current and memory effects. The long delay in turn-off response has been attributed by many to majority carrier traps that are relatively shallow, small electron capture cross-section coupled with large hole capture rate [63,65] and unique potential barriers [66]. Munoz et al. [66] argued that the high gain in PC detectors is caused by a modulation mechanism of the conductive volume in the layer. Because carriers are photo-generated, they are spatially separated by potential barriers generated by band-bending associated with surface and bulk dislocations. Carrier recombination and capture are controlled by such potential barriers and an intrinsic, nonexponential recovery process, leading to long delay times and large gains.

Surface-illuminated GaN and AlGaN/GaN *p-i-n* UV photodetectors prepared by reactive molecular beam epitaxy (RMBE) on sapphire substrates have exhibited excellent performance. The *p-i-n* structures are generally grown on C-plane sapphire substrates by plasma-enhanced MBE or RMBE. Figure 10 shows the typical structure along with a schematic cross sectional diagram of the device structure. In the configuration shown, light is coupled from the top. The thickness of the GaN layer can be adjusted for the light to be absorbed entirely in the top *p*-type GaN layer or the lightly and unintentionally *n*-doped GaN layer (referred to as the *i*-layer) or both. AlGaN (AlGaN homojunction), GaN (GaN homojunction), and GaN with AlGaN window varieties have been explored. The GaN homojunction structure reported in

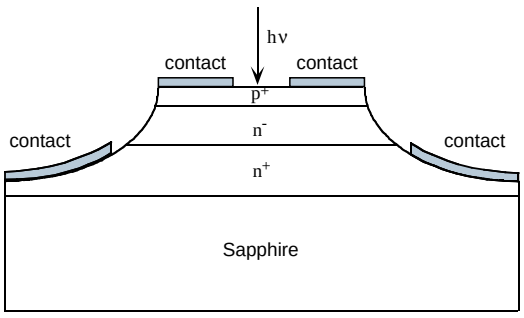


Fig. 10 - Cross-sectional diagram of a typical *p-n* junction UV detector.

Ref. 8 consists of the following layers in growth order: 1) a thin AlN buffer layer, 2) a 3-µm Si-doped GaN *n*-layer, 3) a 1-µm GaN *i*-layer, 4) a 0.2-µm Mg-doped GaN *p*-layer, and 5) a 100 Å AlGaN cap layer. The AlGaN(*p*)-GaN(*i*)-GaN(*n*) (AlGaN/GaN) heterojunction structure consists of the same set of layers as above except that the 0.2-µm *p*-GaN layer was replaced with a 0.2-µm *p*-$Al_{0.12}Ga_{0.88}N$ layer (bandgap ~3.7 eV). Thus, the *p*-layer is transparent to light at the band edge of the GaN *i*-layer. In the device fabrication that followed, the samples were etched down to the *n*-layer, forming 250-µm diameter mesas by a reactive ion etching (RIE) process. The *n*-type contact was made by depositing Ti/Al/Ti/Au multilayers and alloying at 900 ºC for 30 s using a rapid thermal annealing furnace. The Ni/Au ring contacts to the top *p*-layer were then deposited and annealed in a tube furnace at 650 ºC for 90 s in nitrogen.

Figure 11 shows the typical I-V characteristic curves of both the GaN and AlGaN/GaN *p-i-n* devices. It should be noted that the reverse current near-zero bias is limited by the measurement setup. Preliminary measurements indicate the actual current to be several orders of magnitude smaller. The homojunction has a turn-on voltage of 4 V and a reverse breakdown voltage of ~ -100 V, while the heterojunction has turn-on and breakdown voltages of 5.7 V and -50 V, respectively. The increased leakage current in the AlGaN/GaN *p-i-n* device is attributed to the lower quality of the *p*-AlGaN layer as opposed to that of the *p*-GaN layer.

Figure 12 shows the spectral response of a GaN UV detector with an $Al_{0.12}Ga_{0.88}N$ window layer as measured by top illumination at normal incidence for zero bias and -10 V bias. At 364 nm, the spectral bandwidth of the monochromator was approximately 1 nm, and the light intensity on the detectors was approximately 0.06 mW/cm^2. A mechanical chopper modulated the incident light, and a lock-in amplifier recorded the photo current from the *p-i-n* photo diode. A calibrated Si photodetector was used to measure the spectral intensity of the light source and convert the measured detector current to absolute responsivity. As can be seen, the responsivity drops by more than three orders of magnitude as the incident light's wavelength increases from 360 nm to 390 nm. Moreover, reverse bias enhances the response (0.15 A/W at -10 V) while maintaining the sharp cutoff edge and low noise characteristics of the zero-bias responsivity. Under -10 V bias and at 364 nm, the external quantum efficiency is ~51% for the AlGaN/GaN detector and the internal quantum efficiency is estimated to be over 80% considering the surface and interface reflection.

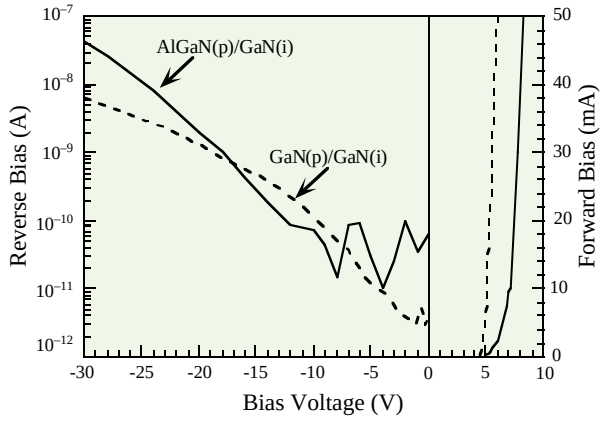


Fig. 11 - Typical I-V characteristics of GaN and AlGaN/GaN *p-i-n* devices.

The rms noise current at 400 nm is approximately 1 pA (limited by the measurement setup), corresponding to an NEP of approximately 8.3 pW. The AlGaN/GaN *p-i-n* device also exhibits higher responsivity in the 260 to 300 nm spectral region of importance. To a first approximation, we observe that the curved shape of the responsivity of the AlGaN/GaN

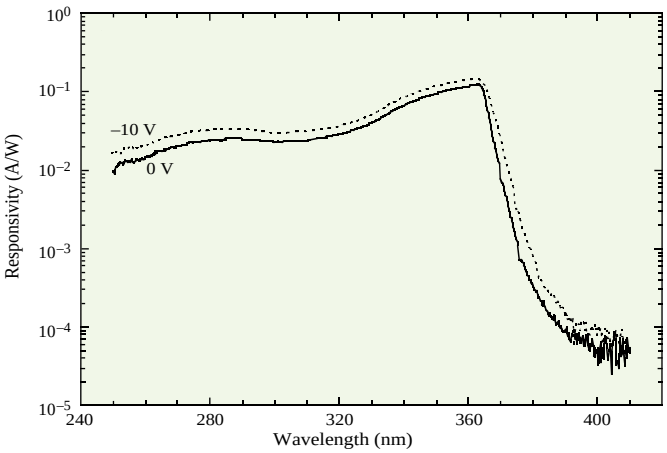


Fig. 12 - Spectral responsivity for an AlGaN-p/GaN *p-i-n* photodetector under zero bias (0 V) and -10 V reverse bias.

p-i-n in the 260 to 300 nm spectral region is similar to that of the GaN *p-i-n* but blue-shifted to the AlGaN bandgap. When the defect concentrations in layers are reduced, biased operation and designs that allow absorption in the *i*-layer would increase the sensitivity and the speed of response somewhat. The AlGaN *p*-layer is much desired since it is transparent to the light at the GaN bandgap. Ideally what this means is that photons with energies below that of the AlGaN bandgap would be absorbed in the *i*-layer, where they would generate carriers, that in turn, would be swept by the electric field. For photons with energy greater than that of the bandgap of the *p*-layer, excessive absorption in the top layer is still a problem that is exacerbated by the small diffusion coefficient (about 0.1 µm).

An equally important figure of merit for a photodetector is its speed. The time response for the devices incorporating several design features such as all GaN, all AlGaN, and heterojunction types at zero bias were measured at 355 nm using a pulsed-nitrogen laser and by monitoring the decay of the photocurrent. The exponential decay times of the photocurrent of the GaN, $Al_{0.05}Ga_{0.95}N$/GaN, and $Al_{0.1}Ga_{0.9}N$ *p-i-n* were found to be about 29, 22, and 12 ns, respectively, as shown in Fig. 13. Fall times as low as 6 ns have been measured [67]. Generally, detectors exhibit two regimes in the photocurrent time decay. At high excitation intensities, trap states in the GaN bandgap presumably become saturated and the detectors are then capable of resolving the 8 ns excitation pulse. At lower excitation intensities, a longer time response tail dominates the decay. In this regime, the detectors have a rise time of less than 5 ns and a fall time (1/e) of approximately 31 ns.

Noise characteristics of the three types UV detectors (GaN homojunction, $Al_{0.03}Ga_{0.97}N$ homojunction, and $Al_{0.1}Ga_{0.9}N$ / GaN heterojunction devices) measured by the group of Prof. H. Temkin at Texas Technical University are plotted in

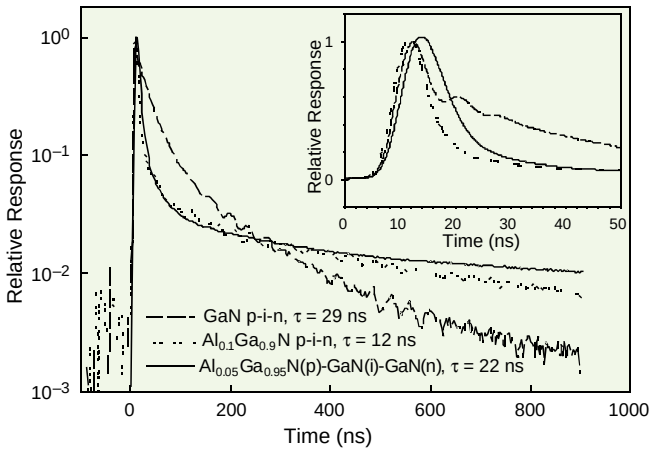


Fig. 13 - The time decay of the photo current for GaN, $Al_{0.1}Ga_{0.9}N$/GaN, $Al_{0.1}Ga_{0.9}N$ *p-i-n* detectors [67].

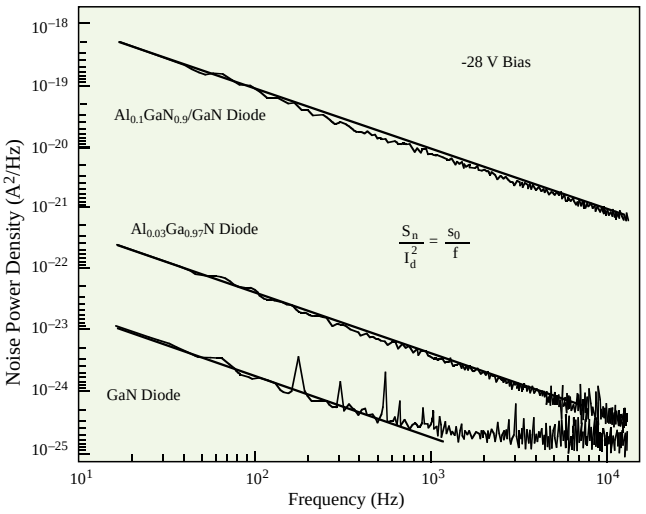


Fig. 14 - Noise power density measured at -28 V for three different diodes, measured by the group of Prof. H. Temkin at Texas Tech University.

Fig. 14, while the noise parameters are tabulated in Table 2. Detector noise for all three devices for small bias values was below the noise floor of the measurement setup. Hence, the noise characteristics were measured at a reverse bias of 28 V. Also tabulated is the corner frequency f_c (i.e., the frequency where the 1/*f* noise density is equal to the shot noise density). The NEP is then found as usual, by calculating the total rms noise current and dividing it by the responsivity of the device.

Despite the remarkable developments detailed above, true solar-blind detectors with very low noise levels and signal amplification have not yet been reported. The ternary AlGaN with large AlN mole fractions would have to be prepared with high quality. If *p-n* junction varieties are to be used, high *p*-doping in such a high mole fraction AlGaN is no easy task and none has been demonstrated. Schottky barrier varieties may remove the requirement of *p*-doping. However, if avalanche photo diodes are pursued for their much-needed gain, as required by systems applications, the Schottky

Table 2 - Noise Data for GaN Homojunction, $Al_{0.03}Ga_{0.97}N$ Homojunction, and $Al_{0.1}Ga_{0.9}N$/GaN Heterojunction Devices

Parameter	GaN Diode	AlGaN Diode	AlGaN/GaN Diode
I_d @ –28 V	5 nA	7 nA	7 nA
I_d @ –2 V	7 pA	7 pA	7 pA
f_c	158 Hz	1638 Hz	1638 Hz
NEP (total)	1.18×10^{-11} W	9.1×10^{-12} W	2.06×10^{-11} W
NEP @ 10 kHz	2.14×10^{-14} W/Hz$^{1/2}$	1.25×10^{-14} W/Hz$^{1/2}$	2.49×10^{-14} W/Hz$^{1/2}$

Notes: 1) Bandwidth was assumed 30 MHz for GaN and 50 MHz for AlGaN diodes
2) Responsivity was assumed 0.07 A/W for GaN and 0.12 A/W for AlGaN diodes
3) I/f noise power density at 1 Hz is 8×10^{-18} A^2/Hz for the $Al_{0.1}Ga_{0.9}N$/GaN diode, 3.8×10^{-21} A^2/Hz for the $Al_{0.03}Ga_{0.97}N$ diode, and 1.8×10^{-22} A^2/Hz for the GaN diode

barrier varieties may not be as successful as the *p-n* junction varieties have been in avalanche photo diodes based on conventional compound semiconductors. Moreover, very little is really known about the ionization coefficients of electrons and holes in GaN and its alloys. The calculations are frustrated by the lack of reliable data on the properties (such as complete band structure) of these materials. These difficulties should, however, be viewed as challenges rather than obstacles as has been the case for just about any advancement. A reasonable midway set of performance goals would be to achieve near 80% to 90% internal efficiency, 10^{-14} W NEP, higher than 100 MHz frequency response, 260 to 290 nm wavelength response, and 10^{-4} of peak response relative response at 300 nm for AlGaN detectors.

Table 3 presents a no-doubt incomplete collage of various UV detectors for comparing and appraising the state-of-the-art. What can be discerned is that the recent progress is extraordinary and that MBE-prepared detectors are very competitive with MOCVD-fabricated detectors despite the scant activity. The last row in Table 3 (i.e., for the PMT-based imager) indicates the possibilities of the hybrid approach used by the Lockheed-Martin Company.

The single-pixel detector development is beginning to give way to arrays for imaging. By combining the spectral signature and image of the source, one can more definitively identify the origin. For example, an 8×8 GaN Schottky barrier photo diode array for UV imaging having pixel sizes of 200 μm × 200 μm, and responsivity of 0.06 A/W has been reported [76]. A purportedly RC time-limited speed of response of 50 ns was reported. In another effort, a 1×18 GaN MSM linear array with a responsivity of 3250 A/W at a bias of 10 V with a response time of 0.5 ± 0.2 ms was also reported [77].

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Table 3 - Comparison of the Performance (Responsivity, R, Internal Gain-Quantum Efficiency Product, G·η, NEP, and Photocurrent Decay Time, τ) of some State-of-the-Art III-Nitride Photodetectors

Detector	*R* (A/W)	G·η (internal)	NEP (W)	τ (s)	Ref.
$Al_x Ga_{1-x}N$ PC	18-300	64-1500		$1\text{-}2 \times 10^{-3}$	68
$Al_x Ga_{1-x}N$ PC	$0.035\text{-}2.8 \times 10^{-6}$			$0.13\text{-}0.36 \times 10^{-3}$	69
GaN PC	125	600		$>20 \times 10^{-9}$	70, 71
GaN MSM	0.3		57 pA at 10V		72
n-GaN Schottky PD	0.18		$\sim 7 \times 10^{-12}$	120×10^{-9}	51
GaN *p-n* PD	0.14		7×10^{-14}	1.7×10^{-8}	57
AlGaN/GaN *p-n* PD		0.5		10	73
GaN *p-i-n* PD	0.11	0.48		8.2×10^{-3}	62
AlGaN/GaN *p-i-n* PD	0.15	0.63	8×10^{-12}*	1.2×10^{-8}	8
GaN *p-i-n* PD				9×10^{-11}	74
PMT-based imager	~670	~3000	$\sim 10^{-15}$	$<10^{-3}$	75

*Limited by measurement setup. The total NEP value at a reverse bias of 28 V is 2.06×10^{-11} W.
PC = photoconductor, MSM = Metal Semiconductor-Metal, PD = photodiode, PMT = photomultiplier.

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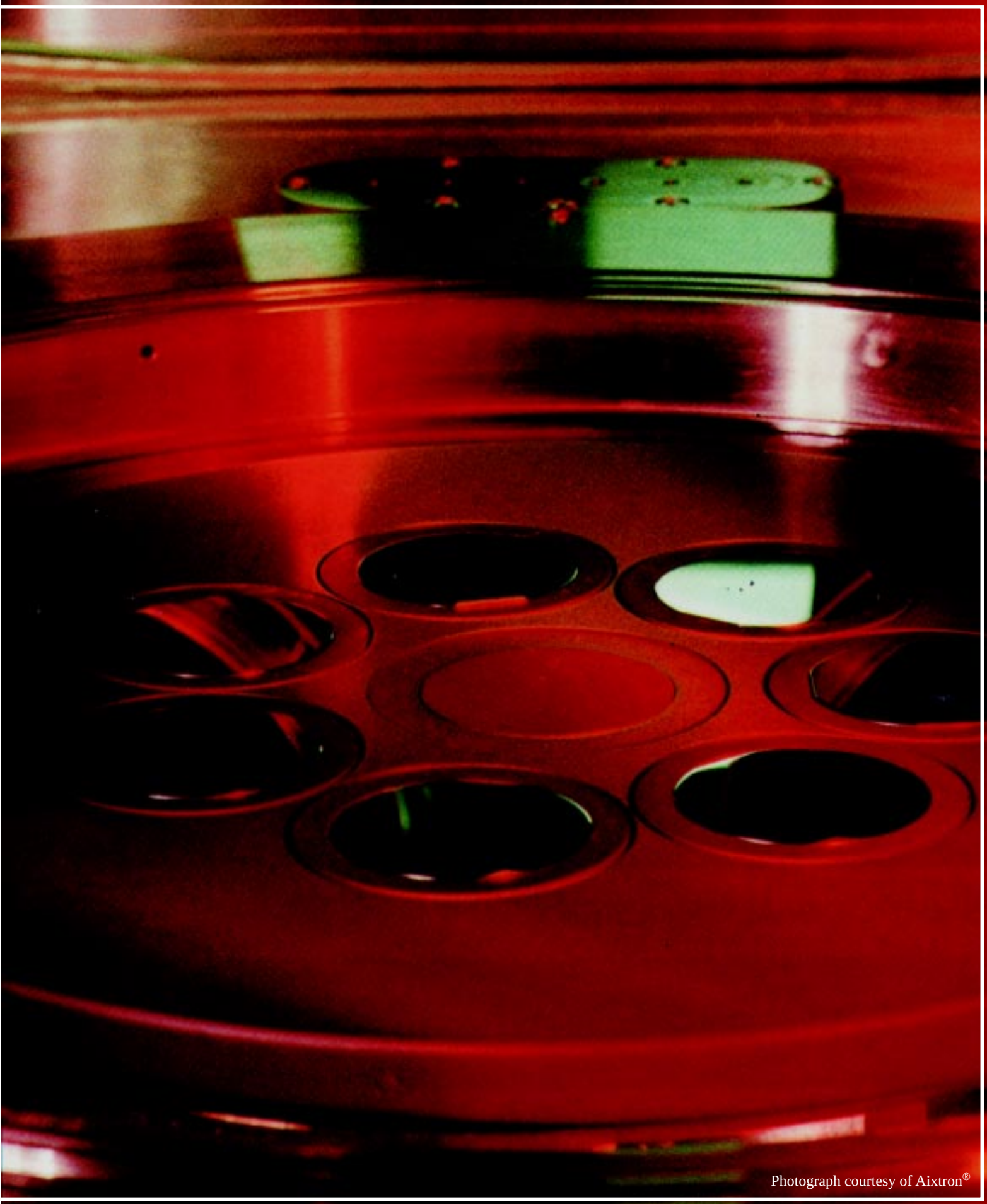
How do they DO that?

Although their potential has been recognized since the 1960s, the Group III-nitrides have trailed way behind the easier-to-grow Si and GaAs semiconductors on the development curve. Ideal substrates upon which to grow the nitrides could not be found, and experiments on existing substrates yielded materials with too high concentrations of defects to afford the desired electronic properties.

Nearly 30 years later, however, Si and GaAs have been pushed to their theoretical limits while GaN and the other wide bandgap semiconductors are just beginning to show their stuff. Why the late blooming? The recent and startling advances in the application of the electronic capabilities of the GaN semiconductors are the direct result of several developments: greater precision in growth techniques; higher purity of chemicals used in film deposition; the development of new techniques for selective deposition of the impurities through which the nitrides get their remarkable electronic properties; and realization of immobile electrical impurities under high applied voltages. One of the most significant insights was that older methods of growing Si and GaAs semiconductors could be applied to producing these materials as well. By using new variations on these already mature technologies, researchers are working to produce GaN thin films on GaN substrates as well as on sapphire and silicon carbide (SiC). They are graduating a class of semiconductors whose performance is expected to drive microelectronic and optoelectronic device capabilities well into the next century. In this article, North Carolina State University materials science and engineering researchers brief us on recent developments in the growth of these materials and deliver an accessible tutorial on the methods, the materials science, and the challenges remaining in producing Group III-nitride thin film semiconductors.

– S.O.



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Recent Progress in the Growth and the Control of Defects and Electronic Properties in III-Nitride Thin Films

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III-Nitride Material Properties

Gallium nitride (GaN), aluminum nitride (AlN), and indium nitride (InN) form a group of wide bandgap semiconductor materials called the Group III-nitrides. These materials have long been recognized for their potential for optoelectronic and microelectronic semiconductor device applications. Substantial research on III-nitride growth was initiated in the early 1960s; however, progress slowed because ideal substrates could not be found and the consequential growth of GaN thin films contained substantial concentrations of defects and lacked the desired electronic properties. These investigations essentially ended in the early 1970s while research on silicon (Si) and gallium arsenide (GaAs) materials advanced rapidly. However, the 1990s have brought significant advances in the sophistication of growth techniques, the purity of the chemicals used for film deposition, the controlled introduction and activation of selected impurities that give the desired electronic properties to these films, and the immobility of the aforementioned defects under an applied electrical voltage. These advances have allowed rapid progress to be made in the III-nitrides.

The III-nitrides possess considerable physical hardness, good thermal conductivity, and high melting temperatures. Ternary alloys of selected fractions of GaN, AlN or InN, and device structures made from layers of these compounds and their alloys can be produced to emit light in colors that span virtually the entire visible spectrum and expand into the ultraviolet (UV) spectra. Green, blue, and UV light emitting devices, UV light detectors, and microelectronic devices for high temperature, high power, and high frequency are representative applications. Recently, III-nitride light emitting diodes (LEDs) have been commercially realized. The range of green-to-UV wavelengths represents a commercially important region of the electromagnetic spectrum. Market projections show that blue and green LEDs will represent the majority of the estimated $3 billion per year GaN-based device market by 2006. The combination of GaN-based blue and green LEDs with gallium arsenide-based red LEDs already forms the basis for large scale, full-color video displays. GaN-based solid-state white light sources with long lifetimes (i.e., more than 100,000 hours) and significantly reduced power consumption requirements offer advantages over incandescent or fluorescent light sources. The demonstration of continuous operation of GaN-based laser diodes (LDs) at room temperature with a projected lifetime of 10,000 hours has been reported [1]. The use of violet or UV LDs in optical data storage applications offers the potential for a fourfold increase over current data storage densities.

Significant progress has also been made regarding III-nitride microelectronic devices; however, continued research is required to achieve commercial viability. High electron mobility transistors (HEMTs) currently comprise the bulk of microelectronic research. These devices take advantage of the thermal, electronic, and piezoelectronic properties of GaN and AlGaN and perform in environments not covered by current technology. Further advances, including novel material fabrication techniques discussed herein, have already increased the capabilities of select III-nitride optoelectronic devices; these techniques will likely have the same positive effect on the microelectronic devices.

During the next decade, the transition of III-nitride materials and related device technologies from laboratory experiments to commercial products will be fueled by recent advances in

the process routes for growth of these materials and the recent realization of commercially viable III-nitride devices. Although III-nitrides are grown using different environmental conditions (e.g., pressures, temperatures, and chemical precursors) than those used for the more developed silicon and gallium arsenide material systems, the techniques used to grow the III-nitride thin films are essentially the same. These scientifically mature growth and deposition techniques as well as the innovative approaches material scientists have recently employed and adapted to overcome many of the difficult obstacles to III-nitride growth are discussed below.

Growth of III-Nitride Thin Films

One of the challenges that faced researchers in the evolution of III-nitride semiconductors was the development of processes to grow the thin films needed for the different types of devices. Single-crystal thin semiconductor films are normally the building blocks for various devices and are achieved via "epitaxial growth." The word *epitaxy* is derived from the Greek word *epi* meaning "*on*" and the Latin word *taxis* meaning "*arrangement*" or "*order.*" Epitaxial growth is a process through which a crystalline substance with a particular arrangement and orientation of atoms is grown upon a crystalline substrate with the same atomic arrangement and orientation. There are two different types of epitaxial growth: homoepitaxy and heteroepitaxy. Homoepitaxy refers to epitaxial growth where the thin film and substrate are the same material. A common example is the growth of a silicon epitaxial layer on a silicon substrate or wafer. Heteroepitaxy refers to the epitaxial growth of dissimilar materials. Gallium nitride growth on sapphire or silicon carbide is an example of this type of growth. Epitaxially grown sequences or multiple layers of thin films, sometimes called heterostructures, form the basis of many different types of semiconductor devices.

Many epitaxial thin film growth processes have been developed, including molecular beam epitaxy (MBE), hydride vapor phase epitaxy (HVPE) and metalorganic vapor phase epitaxy (MOVPE), and derivatives of these methods. The MOVPE technique is commonly used for the heteroepitaxial deposition of compound semiconductors, including III-nitride thin films. Characteristics of this method include the use of high purity chemical sources, a high degree of compositional control and uniformity, high growth rates, and the ability to grow abrupt junctions.

Growth of GaN thin films using MOVPE is achieved at temperatures ranging from 900 to 1100 °C (1655 to 2015 °F) via the introduction of gases into a specially designed reaction chamber at specific rates and ratios. The reaction chamber is usually maintained at or below a pressure of one atmosphere during the growth process. The gases decompose on the hot substrate and the resulting products of this reaction combine to form the thin film. This chemical reaction must be carefully controlled to obtain optimum film properties. During growth, the deposition conditions can be altered to manipulate the compositions and electrical properties of the film to meet the application requirements for the material and desired device.

Two of the more important crystal properties that must be closely matched between the thin film and substrate are the distances of separation among the atoms at the thin film/substrate interface and the amount of expansion and contraction that occurs during heating and cooling. Any mismatch in these properties can result in imperfections and defects in the thin film. These defects directly affect the success of the fabrication and performance of the final optoelectronic or microelectronic device.

The ideal candidate substrate for the growth of GaN thin films is a GaN wafer. These wafers allow homoepitaxial growth and provide exact matches of the atomic spacing and of the coefficients of thermal expansion between the substrate and thin film. Several research groups are investigating the growth of bulk GaN crystals and very thick films through various techniques; however, commercially available large area GaN wafers appear to be several years away. The wide bandgap semiconductor community is therefore challenged with growth of heteroepitaxial films.

Heteroepitaxial growth of GaN films was initially performed directly on sapphire and silicon carbide substrates. Relatively large mismatches in atom-atom separation between GaN and those substrates made nucleation and growth of thin films difficult. For the growth of the GaN thin film to proceed, the gallium and nitrogen atoms near the substrate interface must shift their positions to accommodate the misalignment and assume the spacing of the substrate. This shift in atomic position results in the formation of crystalline defects that exhibit the characteristic of threading vertically from the substrate interface through the newly deposited GaN thin film. These "threading defects" are detrimental to the performance of optical and microelectronic GaN-based devices.

To reduce the influence of these mismatches in atomic spacing, researchers now employ an intermediate "buffer" layer which is grown on the substrate prior to the growth of the GaN or other III-nitride film. Although the buffer layer has reduced the effects of the atom-atom strain created by

the differences in atomic spacing, the densities of the threading defects in these thin films are on the order of one million times higher than in other semiconductor systems. The dark, vertically oriented stripes visible in the GaN film in the transmission electron microscopy (TEM) image shown in Fig. 1 are these threading defects. Consequently, until recently, the film quality relative to other semiconductors remained poor. In 1997, a method to further improve the quality of the heteroepitaxially grown GaN by a marked reduction in defect density was employed for GaN films, as discussed in Ref. 2 and in the following paragraphs.

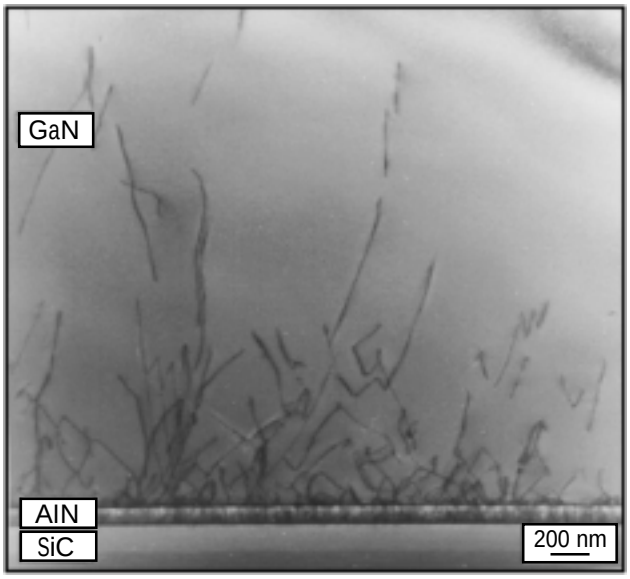

Fig. 1 - Threading defects are seen on this TEM image of GaN grown using an AlN buffer layer on SiC.

Analysis of TEM micrographs of GaN material deposited at NCSU using a technique known as *selective area growth* revealed that certain regions of the film contained a much lower dislocation density (less than 10^4 cm^{-2}) relative to other regions where the dislocation density was approximately 10^9 cm^{-2} (typical of levels found in most GaN films). Selective area growth is not new to the semiconductor industry, having been used often for the growth of silicon and gallium arsenide thin films. In the case of GaN, one approach for this technique employs covering a layer of gallium nitride with a layer ("mask") of silicon dioxide (glass). Small circular or rectangular holes or "windows" are then etched in the mask through which the underlying GaN is exposed. A GaN film is subsequently regrown under conditions such that growth occurs epitaxially only in the windows and not on the silicon oxide mask. Figure 2 shows a scanning electron micrograph (SEM) of the resulting growth within circular holes. These are hexagonal pyramids that have an ideal shape for a microelectronic device known as a field emitter.

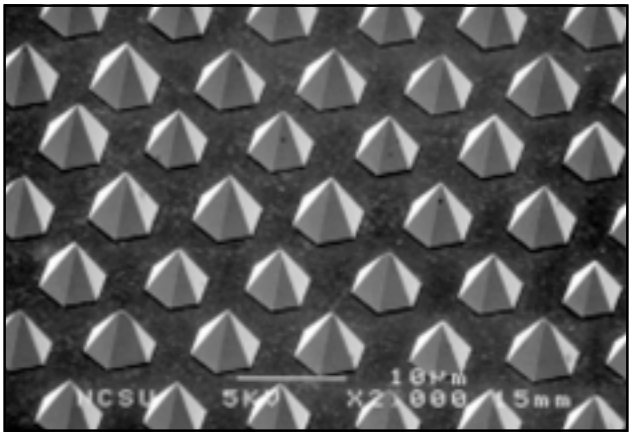

Fig. 2 - SEM image of GaN hexagonal pyramid array.

If the regrowth of GaN is allowed to continue, eventually lateral growth over the mask occurs. This is shown schematically in Fig. 3; a TEM image of typical LEO growth (defined below) is shown in Fig. 4. Analysis of these films revealed that the threading defects were only present in the window regions of the regrown film. Very few threading dislocations were visible in the regrown GaN that extended laterally over the mask.

By using a selected orientation of the rectangular windows, growth temperature, and gallium precursor flow rate, a continuous, coalesced layer of GaN (shown schematically in Fig. 5) containing a drastic reduction in threading dislocations compared to conventional growth can be obtained, as seen in Fig. 6. This technique of selective area growth is

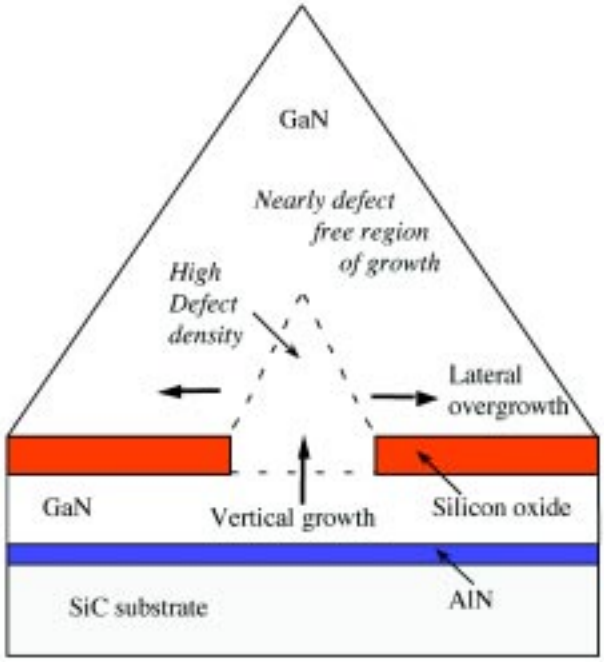

Fig. 3 - Schematic of selective growth.

known as lateral epitaxial overgrowth (LEO). Figure 7 is a color cathodoluminescent image of uncoalesced LEO. The window regions show a yellow-green color due to emission from defects. The overgrown regions show blue color due to an absence of defects. Shortly after these and other observations regarding defect reduction in LEO material were reported, Nichia Chemicals employed the LEO growth technique for their blue laser diodes and announced an increase in device lifetime from a few hundred hours to the estimated and previously noted 10,000 hours [1]. As a result, the LEO technique has received considerable interest from the III-nitride research community.

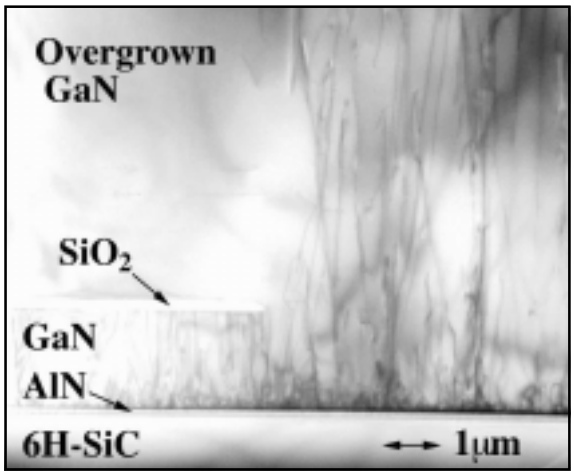

Fig. 4 - Cross-sectional TEM of typical lateral epitaxial overgrowth.

Although the advantage of the LEO growth technique is reduced defect densities, the area of low defect density GaN is confined to strips in the coalesced films over the mask regions. The film over the window regions still contains an unacceptably high level of the threading defects. The result is the disadvantage that the fabrication of semiconductor devices is confined to select areas on the surface of the film. One possible solution to this problem is a reiteration of the LEO process with the second layer translated. Figure 8 is an image of this process obtained using scanning electron microscopy.

In addition to finding new methods to reduce the defect densities stemming from heteroepitaxial growth on sapphire and silicon carbide, researchers have recently renewed their efforts to obtain device-quality, large area GaN films on silicon substrates because of their larger area and lower cost. The disadvantage of using silicon for GaN growth is that the atomic spacing mismatch between GaN and silicon is much greater than that between GaN and sapphire or silicon carbide. Additionally, silicon is not as thermally stable as GaN, sapphire, or silicon carbide, and thus any device application for GaN using silicon as a substrate has limited use. A possible solution meeting all these concerns is to use the LEO technique to grow device-quality GaN on large-area silicon substrates and then remove the silicon substrate from the GaN using established silicon processing techniques.

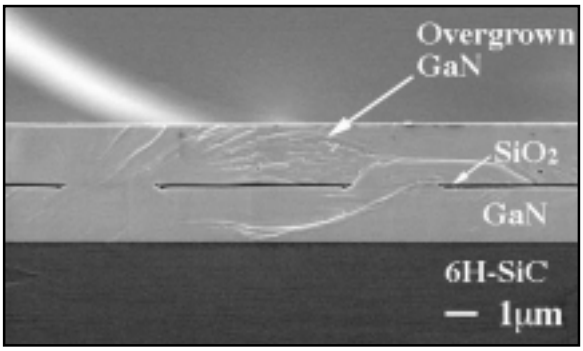

Fig. 6 - Example of coalesced lateral epitaxial overgrowth.

Introducing Impurities to Control Electronic Properties

In addition to growing GaN as well as other semiconductor films with low defect densities, another key requirement for fabricating optoelectronic and microelectronic devices is the ability to precisely control the electrical properties of the thin films. By "using" and "controlling" electrons, we can "communicate" with semiconducting materials and exploit their unique crystalline responses to different "stimuli" (e.g., light, pressure, heat, and electrical voltages and currents). Most materials can be broadly classified using the modern *band theory of solids* as metals, semiconductors, or insula-

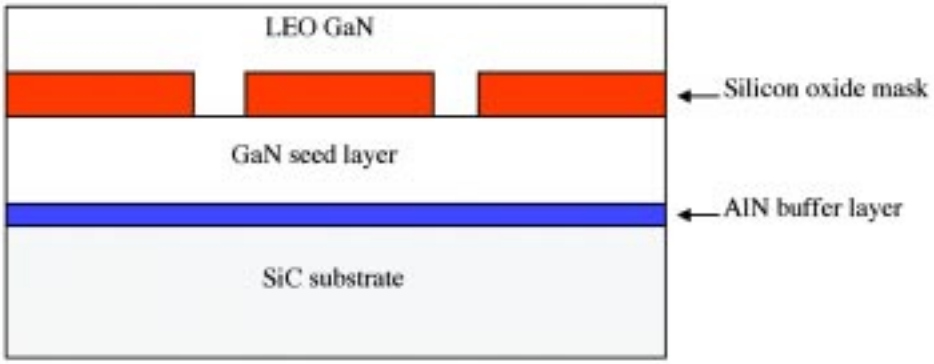

Fig. 5 - Schematic of coalesced lateral epitaxial overgrowth.

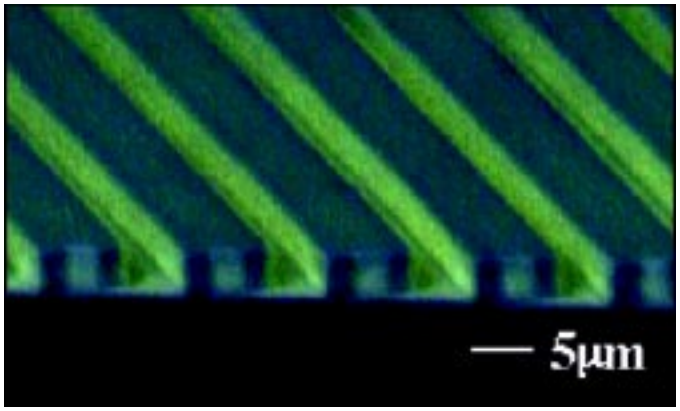

Fig. 7 - Color CL image of lateral epitaxial overgrowth of GaN.

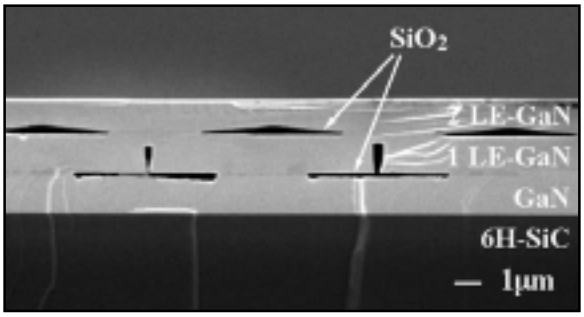

Fig. 8 - SEM image of double layer LEO.

tors. In this theory, the bands consist of electrons that share similar energy levels. In metals, electrons move in the partially filled valence (bonding) band upon the application of a voltage potential and are the charged entities by which an electrical current is achieved and measured. This is referred to as current conduction. In insulators and semiconductors, the valence band is completely filled and, in order for conduction to occur, enough energy must be provided to cause the electrons to jump into the conduction band. The size of the energy gap separating the bands distinguishes insulators from semiconductors: Insulators exhibit very wide energy gaps, whereas semiconductors have energy gaps that span from narrow to wide.

Another form of electrical conduction is found in materials. When an electron moves from the valence band, it leaves behind a vacancy. An electron from an adjoining atom can fill that vacancy, leaving behind a vacancy in the adjoining atom. This vacancy is called a *hole* and acts as another entity that undergoes electrical conduction. However, unlike electrons, holes do not actually carry a charge.

A semiconductor with electrons as the main current conduction mechanism is called an "*n*-type" semiconductor. When a large number of holes are created, holes become the main conduction mechanism in the semiconductor. In this case, the semiconductor is called "*p*-type." The introduction of certain elements into a semiconductor leads to current conduction through either electrons or holes. The careful introduction of these elements into the semiconductor during growth is called *doping*, and allows for control of both the conduction mechanism and conduction level. Many key semiconductor devices, including LEDs and LDs, are based on the positioning of adjacent *n*- and *p*-type semiconductor layers, *p*-*n* junctions, and the resultant electrical properties of the interface between the layers. By controlling the interaction of electrons and holes in the semiconductor, either optoelectronic or microelectronic phenomena result. By controlling the flow of current conduction (by holes, electrons, or both), microelectronic devices such as transistors are obtained. By controlling either the recombination of holes and electrons resulting in light emission or the absorption of light resulting in the production of electrons and holes, optoelectronic devices such as LEDs and light detectors, respectively, are obtained.

The current level of progress in the development of GaN materials and commercially viable devices, namely GaN-based LEDs and LDs, has been the direct result of the relatively recent achievement of *p*-type conduction in GaN. Efficient *n*-type doping of GaN through the use of silicon proved relatively easy to achieve. Doping with magnesium is the most common method of achieving *p*-type conduction in GaN. Initially, MOVPE-grown GaN doped with Mg was not *p*-type, but was highly nonconductive. It was later determined [3] that an interaction between hydrogen and Mg occurred during the growth of the GaN thin films, which created a neutral complex that prevented the formation of holes in GaN. Hydrogen is a gas that is typically present in large quantities in the MOVPE chamber during growth of GaN. Low resistivity, *p*-type Mg-doped GaN was first achieved via post-growth, low-energy electron-beam irradiation, and later through post-growth thermal annealing. These processes dissociated the magnesium and hydrogen in the GaN and allowed *p*-type conduction in the semiconductor.

Summary

Recognized for their stability in harsh environments and their unique electronic properties, the III-nitrides have become one of the few select classes of materials being engineered into optoelectronic and microelectronic devices demanded by today's technologically advancing society. Although early progress was slowed by the lack of ideal substrates and *p*-type doping ability, the pace of successful

III-nitride device fabrication has accelerated within the last few years. Faced with the challenges resulting from heteroepitaxial growth, materials scientists have found innovative ways to improve the crystallinity and to reduce the levels of undesirable and electronically active impurities in GaN and other III-nitride materials. Considerable attention is currently being given to using LEO techniques to drastically reduce threading defect densities that directly affect the operation and efficiency of optoelectronic and microelectronic devices. Having achieved reduced defect densities and *p*-type conductivity, the III-nitride community has finally demonstrated commercially viable GaN-based devices. The first commercially available LED was announced in 1993 [4]. This was followed by the laboratory development of the laser diode in 1996 [1]. An improved version of the LD was fabricated using a LEO base layer in 1997 [5]. Several other investigators have also recently reported successes in fabricating high electron mobility field effect transistors [6-9]. Research regarding the III-nitride materials is now focused on the optimization of these and other devices; thus, methods to improve heteroepitaxial growth and to attain further reduction of the threading defects are once again at the forefront.

Acknowledgments

The authors thank T. Weeks, Jr. and M. Bremser for their assistance in the growth of the materials described in this article and for helpful discussion. We also thank Cree Research, Inc. for the silicon carbide wafers. The NCSU research discussed in this article was conducted under ONR contracts monitored by C. Wood and J. Zolper, respectively. R. Davis was supported in part by the Kobe Steel, Ltd. University Professorship.

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"I'm a

LEO - . . .

grown GaN-based device, which makes me darn near perfect!" might be the boast of a new generation of gallium nitride semiconductor films now being produced and studied in many research programs under the sponsorship of ONR. One such research program is that undertaken at the University of California at Santa Barbara (UCSB) by Dr. Umesh Mishra and his colleagues. The almost dislocation-free GaN thin films they produce by lateral epitaxial overgrowth (LEO) and other techniques hope to become the bases for new devices critical to DoD-required communications and sensing applications. Secure optical communications, wide bandwidth/high power amplifiers, compact power supplies, and solar-blind detectors for, among other uses, missile detection should all benefit in the near term from this research. By detailing the activities underway at UCSB, this article helps to present the story behind the story of the R&D of this promising class of wide bandgap semiconductors.

– S.O.

Gallium Nitride-Based Solutions for Communications and Sensing

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The Department of Defense has an urgent need to reduce the size and increase the sensitivity and efficiency of its communications and sensing systems, and to enhance the system lifetime in hostile environments. The alloy system aluminum-gallium-nitride (AlGaN) offers a unique opportunity to provide a quantum leap in achieving these goals. At UCSB we have had a concerted effort, largely through ONR support, in the areas of

- Blue/UV light emitters (for secure optical communications)
- AlGaN/GaN high electron mobility transistors (HEMTs) (for (a) wide bandwidth/high power amplifiers for reduced radar aperture, and (b) compact power supplies)
- AlGaN/GaN heterojunction bipolar transistors (HBTs; same applications as above), and
- AlGaN solar-blind detectors (for missile detection).

Success in these efforts has in the past relied prominently on our understanding of the growth and doping of these alloys and their heterojunctions, and we anticipate that this will remain fundamental for a few years to come. Continued success of ONR-funded efforts here is based on the unique and close collaboration of faculty from materials growth to circuits and is hopefully apparent in the report.

To explore the great potential offered by the semiconductor material, crystal growth efforts at UCSB were directed towards the synthesis of high quality GaN epitaxial layers and AlGaN/GaN heterojunctions. Besides metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE) has also been applied recently as a growth technique on MOCVD-grown GaN templates. In the MOCVD process, GaN layers were grown on c-plane sapphire, using the precursors trimethylgallium, thrimethylaluminum, and ammonia. Under optimized conditions, GaN films with dislocation densities of 4×10^8 cm^{-2} were obtained, a value which is among the lowest reported for GaN films grown on sapphire. The 300 K electron mobility in 4-μm-thick GaN layers reached values of 820 cm^2/Vs (close to the best reported value of 900 cm^2/Vs by S. Nakamura et al. [1]) and carrier concentrations of $n = 2 \times 10^{16}$ cm^{-3}. The photoluminescence of such films is dominated by band edge emission, even at excitation levels as low as 2.2 mW/cm^2. The GaN surface is atomically smooth and characterized by steps that are one GaN bilayer high.

The MOCVD growth of 20- to 30-nm-thick AlGaN layers on top of semi-insulating GaN films had been optimized with respect to the structural quality of the AlGaN layers and the mobility (μ) and the sheet charge (n_s) of the two-dimensional electron gas (2DEG) forming at the GaN/AlGaN interface. The structural quality of the AlGaN layers depended strongly on the growth conditions and the aluminum composition of the films. Coherently strained AlGaN layers were obtained under conditions ensuring a high surface mobility of adsorbed metal species. Thus, step-flow growth of $Al_xGa_{1-x}N$ up to $x_{Al} = 1$ could be achieved at low ammonia flows during growth (see Fig. 1). Besides the tendency to grow in an island growth mode, AlGaN layers with $x_{Al} > 0.2$ developed stacking fault-related defects, which typically started to form at dislocations. Thus, the formation of these defects could be suppressed by growing on almost dislocation-free laterally epitaxial overgrown (LEO) GaN. The characteristics of the 2DEG were evaluated by Hall measurements after van der Pauw. The mobility of the 2DEG decreased with increasing aluminum mole fraction in the AlGaN layer and increasing surface roughness of the underlying GaN, in agreement with theoretical considerations that suggest a strong confinement of the 2DEG at the interface [2]. For $Al_{0.33}Ga_{0.67}N$/GaN heterojunctions, electron mobilities of 1690 cm^2/Vs at 300 K and 4400 cm^2/Vs at 15 K were achieved. The sheet charge of the

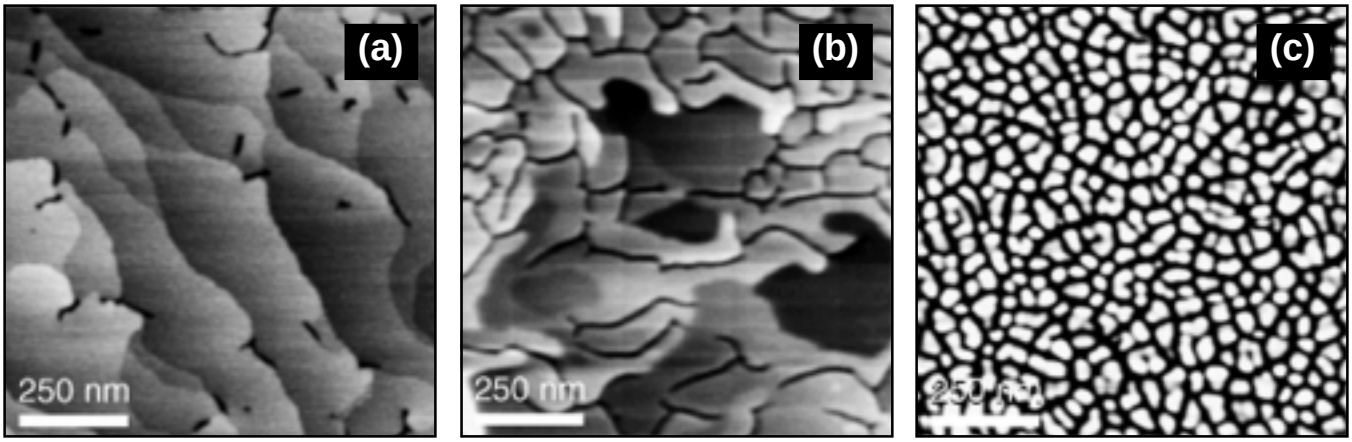


Fig. 1 - Atomic force microscopy images of 18-nm-thick $Al_{0.35}Ga_{0.65}N$ layers grown on GaN by MOCVD with an ammonia flow of (a) 1.5 l/min, (b) 3 l/min, and (c) 6 l/min (grayscale 3 nm). Island growth and defect formation in the AlGaN layer are suppressed at low NH_3 flows during growth.

2DEG was most strongly influenced by the aluminum composition in the AlGaN layer and increased with increasing Al mole fraction due to spontaneous polarization and piezoelectric effects.

AlGaN/GaN HEMTs were fabricated from a variety of wafers. In terms of power density, GaN HEMTs have demonstrated superior microwave power performance compared to gallium arsenide (GaAs) *p*-HEMTs and other conventional III-V devices. UCSB's GaN HEMTs on sapphire substrates have achieved 3.3 W/mm at 18 GHz [3], and just recently the power performance could be improved to 4.2 W/mm at 6 GHz (Fig. 2), which are the highest reported values for GaN HEMTs on sapphire. An even higher power value of 6.8 W/mm at 10 GHz had been recently achieved for AlGaN/GaN HEMTs grown on semi-insulating SiC substrates [4] that, though attractive, are currently in limited supply. To reduce the thermal limitations caused by the sapphire substrate, we chose at UCSB a flip-chip bonding approach of GaN HEMTs grown on sapphire onto AlN substrates [5]. With this approach, 3.2 W output power from a 1-mm wide GaN HEMT was achieved, which is close to the best reported power density for large devices on SiC substrates.

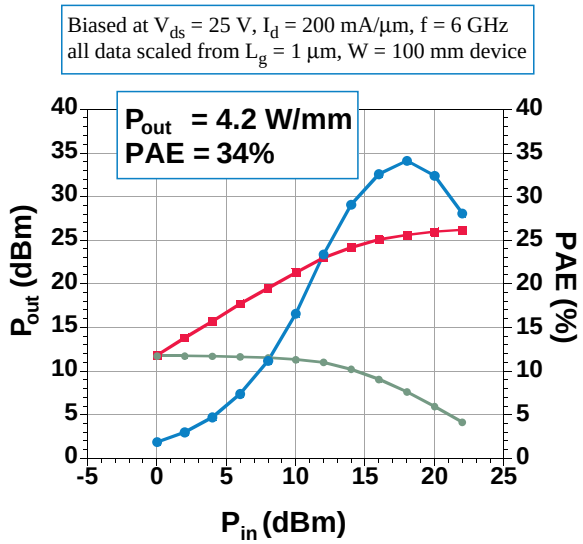


Fig. 2 - Power performance of a GaN HEMT grown on sapphire.

These latest developments in the GaN HEMT device technology enabled the fabrication of the first GaN-based broadband power amplifier with performance superior to that of its GaAs-based counterparts. The modified capacitive-division traveling wave power amplifier (TWPA) circuit topology was chosen in this work (Fig. 3). The amplifier had about 7 dB of small-signal gain with a 3-dB bandwidth of 1 to 8 GHz; both input and output return losses were less than 15 dB. Output power levels of 3.6 W when biased at 18 V and of 4.5 W when biased at 22 V were obtained at mid-band (4 GHz) (Fig. 4). To our knowledge, this is the highest output power for a TWPA using solid-state field effect transistors. The circuit could not be reliably biased above 20 V, however, because of poor wafer uniformity as the device technology is still relatively immature. Much improved performance of the broadband power amplifier is expected with further developments in (Al,Ga)N material growth.

To study the effects of an improved structural quality of the epitaxial layers, AlGaN/GaN HEMTs had been grown on LEO GaN. The LEO technique results in virtually dislocation-free GaN in the overgrown areas (Fig. 5) [6]. While the forward I-V characteristics of devices on regular and LEO GaN were similar, the reduced dislocation density in the LEO GaN had a major impact on the gate leakage: HFETs

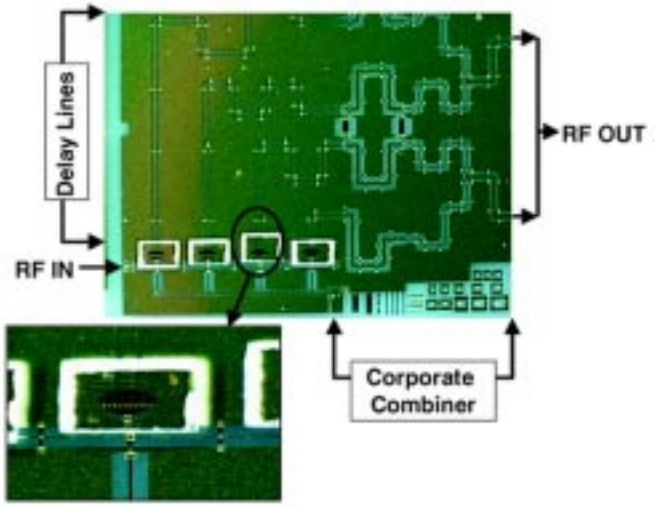
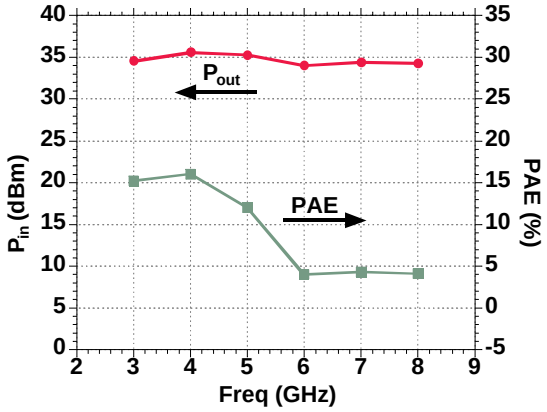
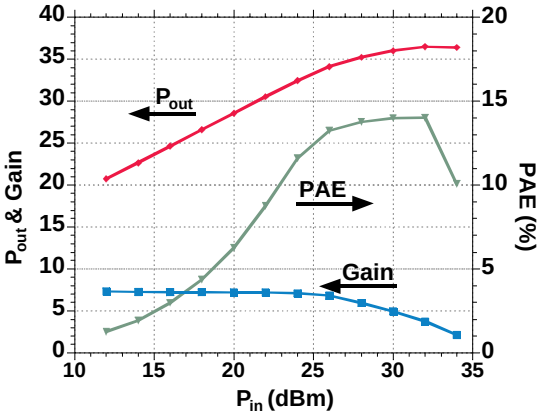


Fig. 3 - First demonstration of a GaN-based broadband power amplifier. Photograph of the fabricated GaN modified TWPA and close-up view of the flip-chip bonded GaN HEMT (the device is visible through the transparent sapphire substrate).



(a)



(b)

Fig. 4 - Device performance of the amplifier: (a) Power vs frequency when biased at V_{ds} = 18 V, class AB mode (b) Power sweep at 4 GHz when biased at V_{ds} = 22V, class AB mode.

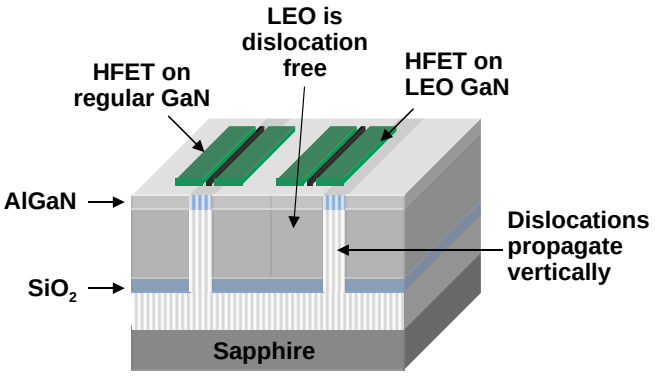


Fig. 5 - Schematic of the AlGaN/GaN HEMT grown on lateral epitaxially overgrown (LEO) GaN. The laterally overgrown regions are virtually free of dislocations.

on LEO GaN consistently showed much lower (up to two orders of magnitude) gate leakage current than HFETs on standard dislocated GaN. Current efforts are directed towards optimizing the growth and coalescence of insulating LEO GaN layers to study the impact of a reduced dislocation density on HFET forward current and transconductance characteristics.

A further area of research has been the development of GaN-based HBTs. In May 1998, UCSB demonstrated the first GaN bipolar transistor (Fig. 6). This device had a DC current gain of three, achieved with a 200-nm base and regrown extrinsic base contacts. The HBT program at UCSB consists of two main objectives: kV range-switching transistors and high-power microwave devices for amplifier applications. Recent devices have been tested with an operating voltage of greater than 100 V. Primary concerns for the progress of the AlGaN/GaN HBT are improving base contact quality and device current gain as well as assessing AC performance. Advances in processing technology have led to an improvement in regrown base contact quality. Also, device structures designed to assess the breakdown voltage of bipolar transistors as a function of collector thickness for use in kV switching devices are being fabricated, as are transistors compatible with AC characterization equipment.

Besides the efforts in the field of electronic devices, UCSB has also demonstrated the first solar-blind (Al,Ga)N-based high-speed UV detector (with a cutoff wavelength of 290 nm or less) that uses a photodiode structure. A key issue in the development of high quality photodiodes is the reduction of defects in the material, particularly threading dislocations. These defects can result in a high leakage current for the devices, which in turn reduces the available signal-to-noise ratio and, hence, the detectivity of the detectors. To reduce the high dislocation density usually present in GaN films, again the LEO technique, with its ability to produce

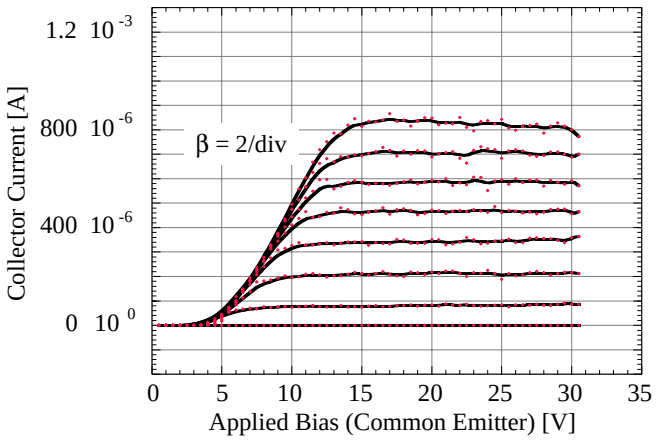


Fig. 6 - First GaN-based HBT. Common emitter characteristics of a 1 μm × 20 μm HBT. The base current was stepped from 0 to 350 μA in 50 μA steps.

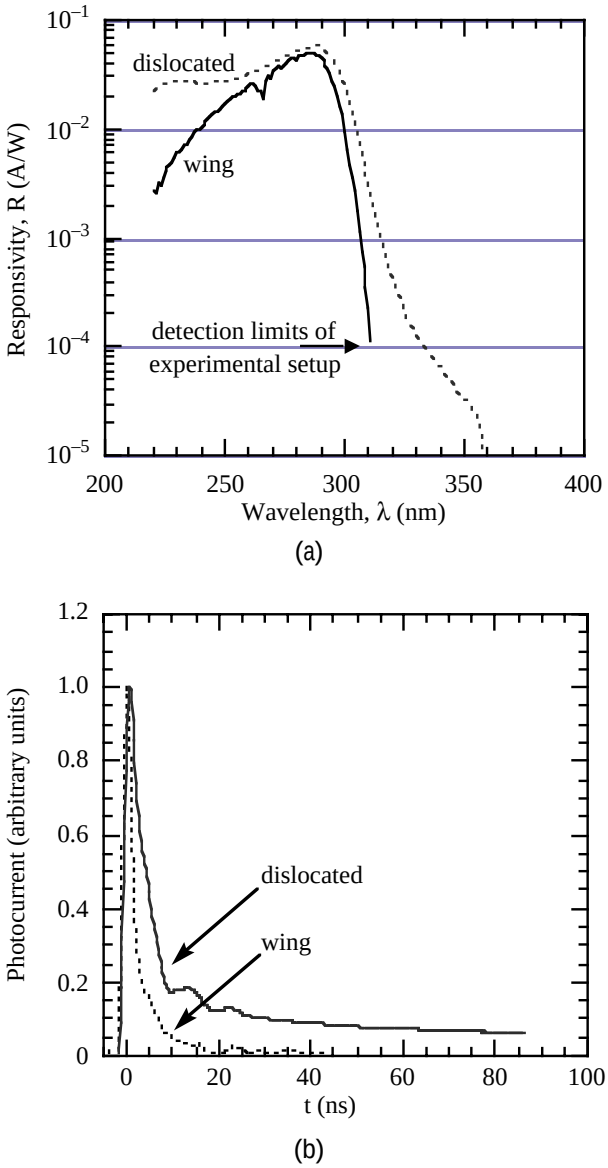


Fig. 7 - First solar-blind high speed AlGaN/GaN photo-diode. (a) Typical pulsed response at 263 nm for diodes fabricated on the virtually dislocation-free wing region of LEO GaN in comparison to diodes fabricated on dislocated GaN. (b) Spectral response curves for diodes fabricated on the wing region of LEO GaN and on dislocated GaN.

virtually dislocation-free overgrown regions, was used. An AlGaN/GaN *p-i-n* structure was deposited on LEO GaN. Photodiodes were then fabricated with the active regions (defined by a 10 μm × 1000 μm mesa) placed so that they were only over the almost dislocation-free LEO wing regions and not the dislocated GaN seed regions. Response times for these diodes were measured to be as low as 4.5 ns for 90%-to-10% decay time (see Fig. 7). Current-voltage measurements of the diodes exhibited dark current densities as low as 10 nA/cm^2 at –5 V on many devices. These current densities were many orders of magnitude lower than those obtained from the same *p-i-n* structure deposited on regular (dislocated) GaN. Spectral response measurements revealed peak responsivities of 0.05 A/W at a wavelength of 285 nm; these were of the same order as the peak responsivities on the equivalent dislocated structure. This indicates a much-improved signal-to-noise ratio for the devices on the LEO GaN. The dislocated devices also exhibited a slower response time and a less sharp cutoff, with significantly more sub-bandgap response.

Recently, also, first experiments to optimize the electrical properties of AlGaN/GaN heterostructures by using MBE as a growth method were undertaken at UCSB. To eliminate problems related to the sapphire nucleation process and the resultant high dislocation and extended defect densities often observed for direct MBE growth of GaN on sapphire, efforts concentrated on homoepitaxial growth on high quality GaN on c-plane sapphire templates grown by MOCVD at UCSB. The studies were performed in a Varian Gen II MBE system. Active nitrogen was supplied by a water-cooled EPI Unibulb Nitrogen Plasma source. Conventional effusion cells were used to provide the Group III elements. On top of an *n*-type GaN MOCVD template, an approximately 250 nm thick unintentionally doped MBE-GaN layer was deposited, followed by ~50 nm of MBE-$Al_{0.07}Ga_{0.93}N$. Temperature-dependent Hall measurements (van der Pauw configuration) revealed mobility values of 14,500 cm^2/Vs at 77 K, and 20,000 cm^2/Vs at 12 K (see Fig. 8), which are the highest reported values for an AlGaN/GaN 2DEG (recently verified at AFRL). Since the sample was grown on an *n*-type GaN template, the room temperature measurements were significantly affected by parallel conduction of low-mobility carriers in the template. Using a

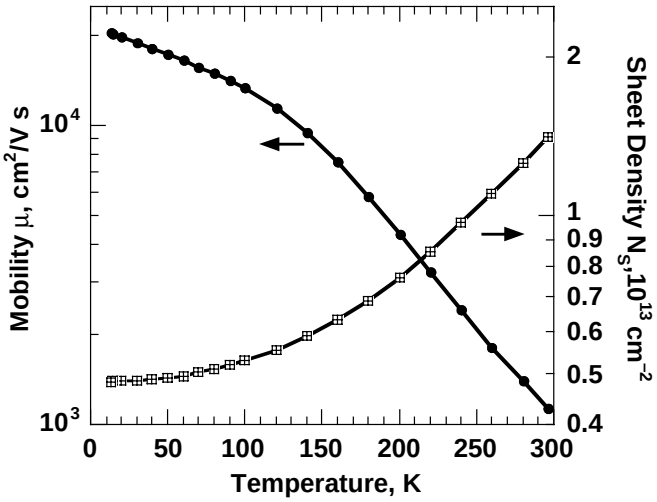


Fig. 8 - World-record 2DEG electron mobility for an $Al_{0.07}Ga_{0.93}N$/GaN heterojunction achieved by MBE growth. Temperature dependence of the electron mobility and the carrier density.

two-layer conduction model, with one layer being the template and the second layer the 2DEG, a room-temperature mobility of 1860 cm^2/Vs and a carrier concentration of 4.8×10^{12} cm^{-2} were extracted. Further MBE growth studies on semi-insulating GaN on sapphire wafers for device applications are under way.

In summary, UCSB's research team of the authors and Professors S. DenBaars, J. Bowers, E. Hu, M. Rodwell, and R. York have undertaken a wide ranging effort to utilize the potential of the alloy system (Al,Ga)N for semiconductor devices, both in the fields of crystal growth and device processing and application of new device concepts. As a result, several AlGaN/GaN-based devices have been demonstrated for the first time. Although the device performance is still limited by the relative immaturity of the semiconductor material, problems have been analyzed and will be addressed in future work.

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growing healthy GaN devices in our Victory Garden

You can give the Naval Research Laboratory a green-thumbs up for its recent harvests of GaN films grown on sapphire substrates. From this remarkable crop, NRL researchers have produced high electron mobility transistor (HEMT) devices that will feed the hungry mouths of DoD's high-end consumers of low-frequency power switching devices, high-frequency microwave radar amplification, and electronic warfare. By cultivating these controllably doped GaN films, NRL is helping to plant the seeds of victory for tomorrow's combatant.

In this article, Dr. Daniel Koleske and other NRL researchers discuss the GaN materials requirements and present a model that shows the required relationship between temperature and V/III ratio for achieving near-stoichiometric GaN growth. They also describe how pressure influences GaN decomposition rate: understanding that is key to weeding out defects and increasing grain size during growth, thus yielding a crop of GaN thin films that have better electronic properties. The authors also give the formula for avoiding those pesky trapping-type defects in GaN MODFET devices. By reducing trapping-type defects in GaN-based devices and otherwise improving GaN thin films, NRL materials scientists are helping the Navy and all of DoD to reap the benefits of its research seed money.

– S.O.

GaN-Based Materials Growth for Microwave Electronic Device Applications

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Introduction

GaN-based electronic devices have demonstrated excellent potential for meeting future Navy needs in microwave radar, electronic warfare, communications, and power switching. Recently, Sheppard et al. [1] have demonstrated working devices with an output power density of 6.8 W/mm and larger devices with a total power output of 9.1 W (3 W/mm). Despite this success, a number of growth and fabrication-related issues remain that must be solved before these devices are inserted in the Fleet.

Many of the growth-related issues emanate from the lack of a suitable substrate for GaN growth. GaN thin films are typically grown on sapphire or silicon carbide (SiC), which do not lattice match GaN well. Because of the mismatch, GaN has a large number of defects and dislocations. However, in working GaN-based LEDs, the dislocation density can number as high as 10^{10} cm^{-2} [2], demonstrating that usable devices can be fabricated. Until GaN substrates are available (which is not likely in the next 5 years), most GaN growth efforts will be aimed at further reduction of defects to improve device performance.

The link between material quality and device performance has been demonstrated in the work of Shuji Nakamura and coworkers at Nichia Chemical Industries, Ltd. Nakamura began work on GaN growth in 1989, which led to the invention in 1990 of a reactor specifically for nitride growth [2]. After his invention, Nakamura quickly demonstrated world-record, 300 K electron mobilities of 930 $cm^2V^{-1}s^{-1}$. In 1994, Nakamura demonstrated a 2-candella blue LED [2], and in 1998 a commercial blue laser [3]. It was the early success in high-quality GaN growth that led to these device successes.

At NRL, we have a focused program in the growth, characterization, and fabrication of GaN-based microwave devices. This in-house capability allows accelerated development of our materials and devices to meet emerging Navy device requirements. In this article, we highlight some of our recent work that has focused on the MOVPE growth of high-quality GaN films and methods to reduce defects in GaN.

Types of Devices and Materials Requirements

For microwave power operation, the primary emphasis is on the development of the high electron mobility transistor (HEMT) structure, as shown in Fig. 1. The active region of this device is a thin conducting GaN layer, which is created by placing a thin AlGaN (20 to 30 nm) layer on the insulating GaN layer. The AlGaN layer creates a 2-dimensional electron gas (2DEG) in the GaN region (denoted by the dashed line) near the AlGaN/GaN interface. In optimized

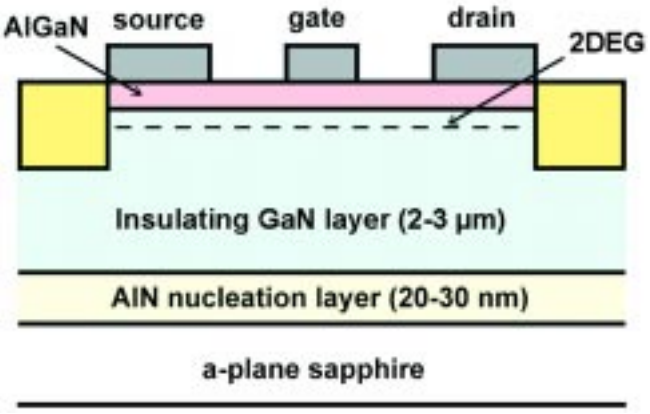

Fig. 1 - In this AlGaN/GaN HEMT device cross section, the yellow area represents the proton-implanted regions.

AlGaN/GaN films, we have recently achieved electron mobilities as high as 1530 $cm^2V^{-1}s^{-1}$ at sheet carrier concentrations of 1.2×10^{13} cm^{-2}.

The most stringent requirement for the HEMT structure is the growth of high quality, insulating GaN. In addition to being insulating, these layers must have high electron mobility when the AlGaN layer is placed on top. Defects located in the insulating GaN layer have been shown to restrict electron conduction through the device layer. Because the quality of the insulating GaN layer has been shown to play a role in microwave device performance, we are focusing on the growth of high quality, insulating GaN.

In 1995, NRL researchers showed how trapping-type defects influence the characteristics of GaN-based devices [4]. An example of trapping-type defects limiting the power performance is shown in Fig. 2 [5]. Each of the HEMT devices in Fig. 2 has similar DC and small-signal characteristics; however, for each device, the drain current responds differently when short (< 1 μs) gate-voltage pulses are applied. Due to trapping effects, devices that have a poor pulse response characteristic (i.e., low I_{pulse}/I_{dc}) also have lower power output, as shown in Fig. 2. The lower current measured under pulse conditions can be attributed to the time dependence of the trapping mechanism. Under microwave test conditions, this trapping mechanism prevents the drain current from responding to the applied gate signal, resulting in lower power output.

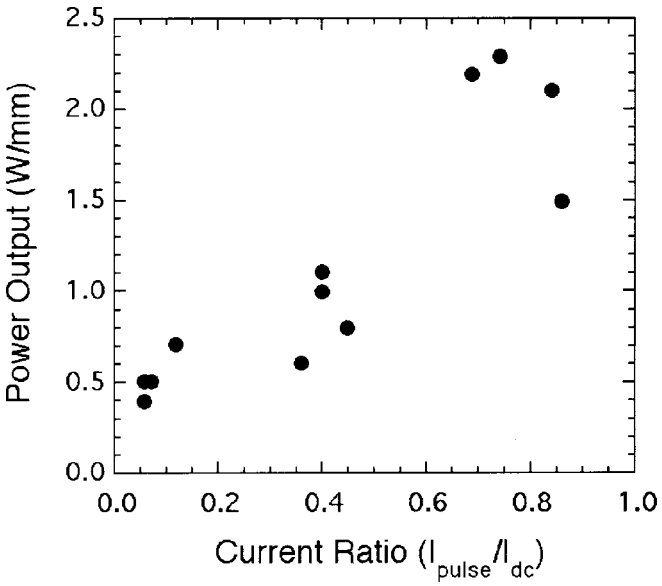

Fig. 2 - The figure shows the correlation of microwave power output at 2 GHz with drain current response to gate voltage pulses shorter than 1 μs. The gate voltage is pulsed from a level less than the threshold voltage to 0 V. The drain voltage is maintained at a fixed value.

Traps also reduce drain current at low voltages leading to current collapse in the device. This is shown in Fig. 3, where the drain current is plotted vs voltage in the dark (dashed lines) and under white light illumination (solid lines) [6]. The low voltage current collapse (in the dark) is consistent with electron trapping in the insulating GaN layer. The trapped electrons form a space charge region at the bottom of the conductive channel, pinching off the device and limiting the current flow through the device. With the light on, the electrons are excited out of these trap states and the space charge region does not develop. As a result, a normal set of drain characteristics is measured. From these examples, it is evident that trapping-type defects play a role in limiting the performance of GaN-based microwave devices.

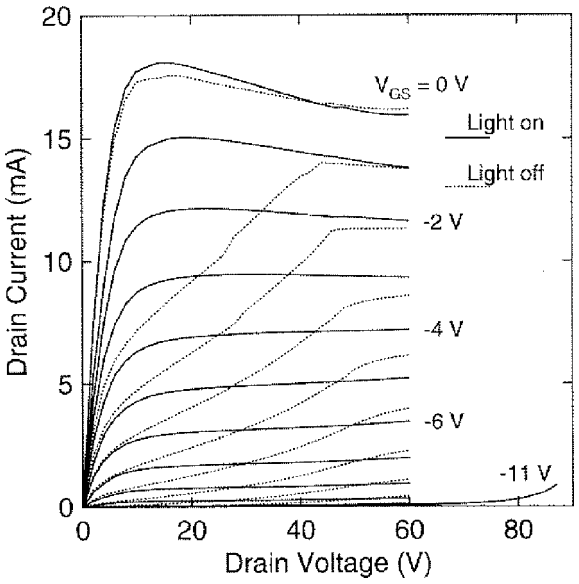

Fig. 3 - Drain current is plotted as a function of the drain voltage with white light illumination (solid lines) and in the dark (dashed lines). In the dark, the drain current collapses for drain voltages less than 50 V are evident after the first curve is measured.

GaN Growth on Sapphire

Prior to the 1990s, there was little interest in GaN as a viable semiconductor, because of the large number of *n*-type defects, low electron mobilities, and rough surface morphology. This changed by 1990 because of the discovery of improved GaN growth on low-temperature AlN nucleation layers (NL) deposited between sapphire and GaN [7]. With the NL innovation, smooth GaN films with improved structural and electrical properties were produced. Using MOVPE growth, GaN films can be grown *n*-type with high mobility, which is ideally suited for LEDs and lasers [2], or insulating, which is ideally suited for microwave FET devices.

In typical GaN films, the electron mobility drops as the *n*-type carrier concentration drops below 10^{17} cm^{-3}. The classical explanation for this observation is that the material is compensated with acceptor-type point defects. Another proposed explanation is that the electron mobility drops because the electrons scatter at the grain boundaries [8]. Both descriptions probably apply to GaN because GaN films are composed of individual grains and contain deep donor and acceptor levels. The GaN grain structure is shown in Fig. 4. The grains can be tilted with respect to the sapphire normal (c-axis) and the grains can also be rotated about the c-axis. Typically, this degree of disorder in semiconductors leads to atomic miscoordination in the lattice, which results in energy levels in the bandgap.

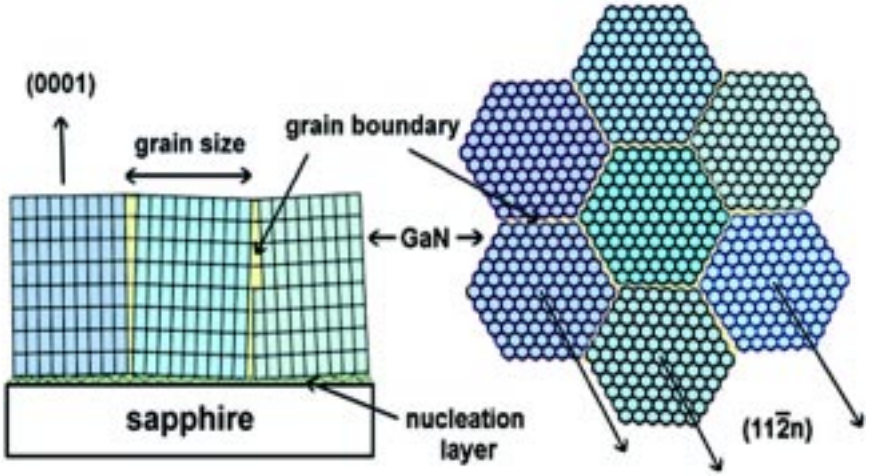

Fig. 4 - This GaN microstructure shows the ordered polycrystalline structure of the individual GaN grains. The side view (a) shows the relative tilt of each grain, and the top view (b) shows the twist of the grains with respect to one another. Edge-type dislocations mainly originate at the grain boundaries, while screw-type dislocations are generally found throughout the entire GaN film (modeled after Hersee [7]).

Because of the presence of grain boundaries, a similarity has been suggested in the electrical conduction between GaN films and polycrystalline Si (poly-Si) [8]. In models developed to explain hole conduction in poly-Si, it was shown that poly-Si behaves like single crystal Si when the doping level is substantially larger than the trap density [9]. However, when the doping and trap densities are similar, the hole mobility drops and the resistivity increases by orders of magnitude. In a similar way, deep level acceptor concentrations in GaN in excess of the shallow donor concentration could cause the resistivity to increase and the mobility to drop. At a fixed trap density in poly-Si, the transition from high mobility to high resistivity shifts from higher to lower dopant concentration as the grain size increases. For poly-Si it has been shown that increases in grain size directly correlate with improved hole mobility. Similar correlations between increased grain size and improved electron mobility have been observed in other polycrystalline compound semiconductors [10].

Toward Defect and Trap Identification and Reduction in GaN

To improve the GaN films, our objectives, presented in the following subsections, include developing growth methods to reduce off-stoichiometric-type defects in GaN, reducing misorientation in our GaN films, and increasing the GaN grain size. In addition, we are working to reduce trapping-type defects, to identify these defects in fabricated GaN devices, and to design vertical GaN-based devices.

Kinetic Model to Explain Stoichiometric GaN Growth

In this section, we show how two growth parameters, growth temperature (T_G) and the V/III ratio (the ratio of N to Ga), are linked to each other and to the resultant GaN quality. Figure 5(a) is a view of one of our MOVPE reactors. The reactor has a showerhead for the separate delivery of the trimethylgallium (TMGa) and ammonia (NH_3) reactants. Since reactor designs vary widely for GaN growth, a more fundamental understanding of the GaN growth chemistry is required. This understanding would facilitate the GaN process development independent of reactor geometry.

Figure 5(b) shows five reaction steps important to growth. These include 1) adsorption and decomposition of the reactants to the growth species, 2) desorption, 3) surface diffusion, 4) incorporation into the solid, and 5) decomposition of the solid. Each of these reaction steps and their relevance to GaN growth are detailed in a recent article [11]. The primary finding in this article is that near-stoichiometric GaN growth can be achieved when the reactant flux ratio of NH_3 to TMGa (i.e., F_{NH3}/F_{TMGa} or V/III ratio) is equal to the N to Ga desorption ratio (i.e., k_N/k_{Ga}). Since the N and Ga desorption rates depend exponentially (Arrhenius behavior) on temperature, their ratio (i.e., k_N/k_{Ga}) also depends exponentially on temperature. When $F_{NH3}/F_{TMGa} \approx k_N/k_{Ga}$ is used for GaN growth, the N and Ga surface concentrations are close to stoichiometric [11].

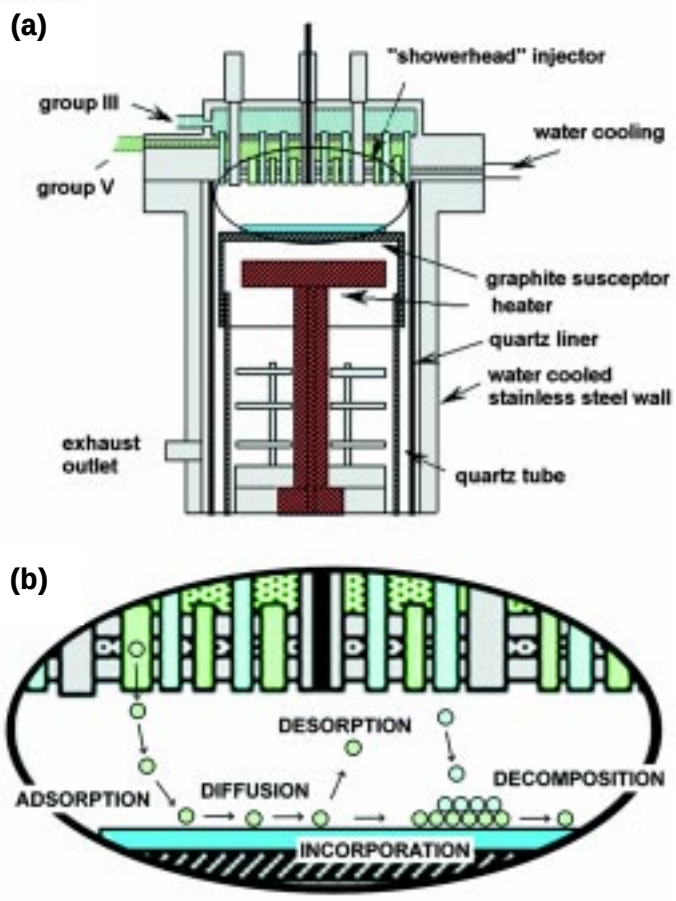

Fig. 5 - (a) Side view of the close-spaced showerhead reactor. This reactor is one of the two MOVPE reactors currently used at NRL for the growth of GaN. (b) The individual reaction steps considered for the kinetic model [11].

This model explains many GaN growth properties. For example, it explains the transition from smooth to rough morphology. Figure 6(a) presents Normarski pictures of both smooth and rough GaN surface morphology. The solid line in Fig. 6(a) is the N to Ga desorption ratio, k_N/k_{Ga}. The V/III ratio and T_G from four growth runs are plotted in Fig. 6(a). For these runs, the V/III ratio (i.e., F_{NH3}/F_{TMGa}) was varied at T_G = 1040 °C. Three of the growth runs had a smooth surface morphology (blue circles), while one of the runs had a rough surface morphology (the red square). Note that growth conditions (i.e., V/III ratio and T_G) that produced the smooth morphology films are all above the k_N/k_{Ga} line, while the growth condition for the rough morphology film falls below the k_N/k_{Ga} line. The surface morphology becomes rough because not enough N is on the surface and Ga droplets form.

When the growth conditions used by other researchers are compared with the k_N/k_{Ga} line in Fig. 6(b), the line properly describes the transition from smooth to rough morphology. As in Fig. 6(a), the red squares denote growth conditions resulting in rough morphology, while the blue circles denote growth conditions resulting in either smooth surface morphology or optimized film growth. Note that all but three of the smooth morphology growth conditions (blue circles) are above the k_N/k_{Ga} line, while all of the rough morphology growth conditions (red squares) fall below the k_N/k_{Ga} line.

Figure 7 compares the optimized V/III ratio and T_G from five different groups to the k_N/k_{Ga} line (blue circles). For each of these points, the V/III ratio and T_G were independently varied to determine the optimal growth conditions. As shown in Fig. 7, the optimized values of V/III ratio and T_G correlate well with the k_N/k_{Ga} line, demonstrating that $F_{NH3}/F_{TMGa} \approx k_N/k_{Ga}$ for optimized growth. Since different MOVPE reactors were used for each of five data points, the GaN growth model developed at NRL satisfies one of our goals, namely to show how the GaN growth parameters

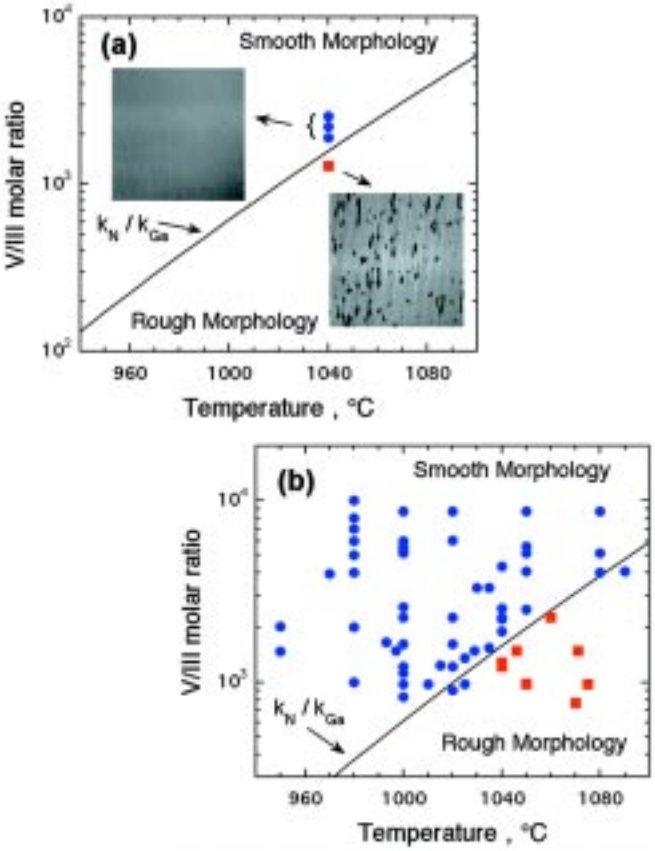

Fig. 6 - (a) The values of the V/III ratio and growth temperature are shown with pictures of the resulting surface morphology. The filled blue circles denote smooth morphology, and the red squares denote rough morphology. The solid line is the k_N/k_{Ga} desorption ratio line. (b) Similar to plot (a), except that the smooth morphology or optimized growth conditions (blue circles) and rough morphology film (red squares) from over 43 literature references are plotted [10].

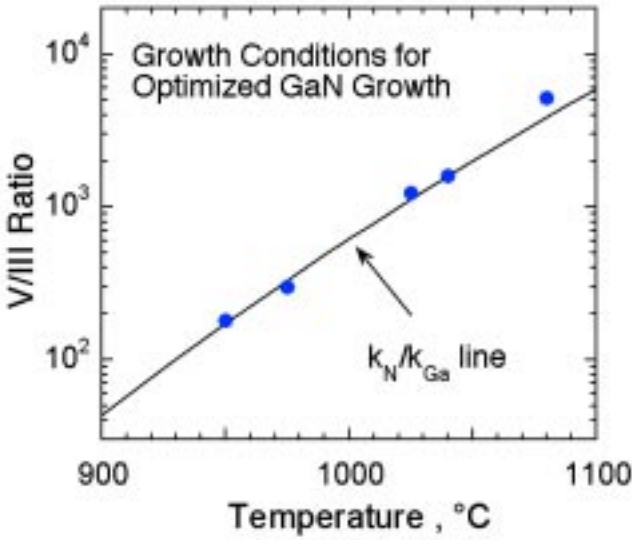

Fig. 7 - The values of the V/III ratio and growth temperature for optimized GaN film growth from five different groups are compared to the k_N/k_{Ga} desorption ratio line.

must be selected with respect to one another independent of reactor design.

Study of GaN Decomposition

The MOVPE growth of GaN is conducted at temperatures that typically range from 900 to 1100 °C. High temperatures are necessary to dissociate NH_3 and form atomic N at the growth surface. This temperature range is substantially higher than the onset temperature for GaN decomposition, which has been reported to be as low as 600 °C. In early GaN growth studies, GaN decomposition was identified as an important chemical reaction detrimental to growth, because it decreases the GaN growth rate.

Recently, we have studied GaN decomposition in flowing H_2, N_2, and NH_3 at MOVPE growth temperatures and pressures [12]. For GaN films annealed in H_2, we found an increase in the GaN decomposition rate by increasing the chamber pressure. Figure 8 plots the GaN decomposition rate (blue diamonds) as a function of total H_2 pressure for 10-min anneals at a temperature of 992 °C. The GaN decomposition rate was found to increase by a factor of 3 when the pressure was increased from 10 torr to 700 torr. At lower temperature, the increase in the decomposition rate vs pressure is even more dramatic. Also plotted in Fig. 8 are the measured rates for Ga desorption (red squares) and liquid Ga droplet buildup (green circles). The droplets increase in size as the pressure is increased, as shown on top of Fig. 8. The increase in the GaN decomposition rate at higher pressures is due to an increased dissociation of H_2, which then combines with surface N to reform NH_3 [13]. At higher pressures, more H_2 is dissociated, which leads to enhanced GaN decomposition.

While detrimental to growth, enhancing the GaN decomposition rate at high pressures brings the growth closer to equilibrium. The enhanced decomposition helps to remove weakly bonded Ga and N atoms, thereby increasing order in the GaN crystal structure. Also, the higher decomposition rate may prevent smaller GaN grains from forming on the NL. As a result, the GaN grain size is increased. The increase in grain size and subsequent improvement in electrical properties at higher pressures has been observed in films grown at NRL (see below) and reported elsewhere [14].

When NH_3 is added to the H_2 flow, the GaN decomposition rate was reduced to 1×10^{17} $cm^{-2}s^{-1}$. This is highly surprising, because GaN growth rates are typically 1×10^{15} $cm^{-2}s^{-1}$ or 1 μm/hour. Put another way, the GaN decomposition rate is 100 times greater than the GaN growth rate. This means that GaN growth is under kinetic control, and this agrees with the initial assertion of the kinetic model described earlier.

GaN Orientation on A-Plane Sapphire

A systematic study was also performed at NRL to optimize the GaN NL in a new close-spaced showerhead reactor geometry [15]. In this study, the sapphire nitridation and low temperature GaN NL were varied. We found that the NH_3 exposure for optimal nitridation depended on the temperature, NH_3 flow, and time. We also found that the nucleation

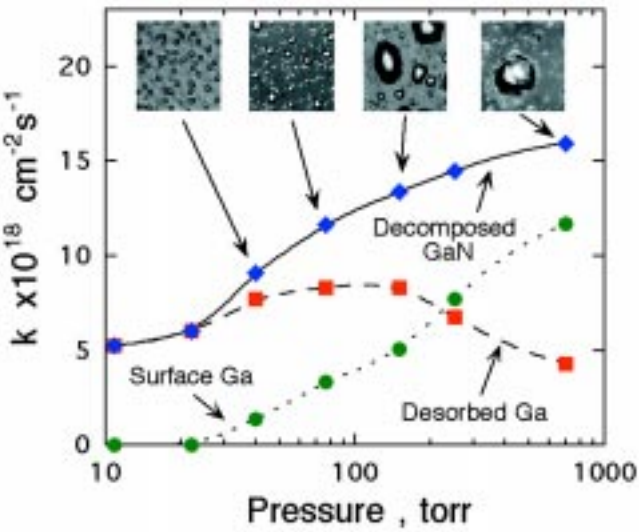

Fig. 8 - The GaN decomposition rate (blue diamonds), Ga desorption rate (red squares), and liquid Ga accumulation rate (green circles) for 10-min anneals in H_2 at 992 ºC are plotted as a function of reactor pressure. Also shown are Normarski phase contrast images of the surface morphology after annealing with arrows indicating the anneal pressure.

site density is strongly influenced by growing the NL at a reduced V/III ratio. AFM and TEM studies of the initial stages of GaN growth on the NL demonstrated improvements in grain orientation as the nitridation and nucleation layer process parameters were varied. For GaN film grown at 76 torr, the electron mobility was 300 $cm^2V^{-1}s^{-1}$ for Si-doped films.

Other work has focused on improving grain alignment by growth on slightly vicinal a-plane sapphire [16]. Hall mobility and X-ray rocking curve data showed a nearly twofold improvement for simultaneous GaN growths on slightly misoriented sapphire compared to on-axis sapphire. TEM revealed a reduction in the edge dislocation density, suggesting better grain alignment on the misoriented substrates, while photoluminescence measurements demonstrated a pronounced decrease in the yellow band emission between the vicinal and on-axis a-plane sapphire substrates. These studies highlight the importance of grain alignment for the growth of high quality GaN.

Development of Large Grain GaN at High Pressure

After optimizing sapphire nitridation and NL growth, GaN growth was conducted at pressures greater than 76 torr [15]. When the NL ramp and GaN film growth were conducted at 150 torr, the electron mobilities were nearly doubled compared to similar growths at 76 torr. A TEM cross section of the GaN film grown at 150 torr is shown in Fig. 9. This film had large grains (4 μm in Fig. 9) and a dislocation density on the order of 10^8 cm^{-2}.

By controlling the sapphire nitridation, NL growth, and growth pressure, we increased the GaN grain. Since the article by Wickenden and coworkers at NRL [15], mobilities exceeding 700 $cm^2V^{-1}s^{-1}$ for Si doping levels of 1.4×10^{17} cm^{-3} have been achieved in the showerhead reactor. In addition, insulating GaN suitable for HEMT development was achieved on AlN nucleation layers. Initial AlGaN/GaN HEMT structures on the insulating GaN have measured 300 K mobilities exceeding 1400 $cm^2V^{-1}s^{-1}$ and sheet carrier concentration of 1.2×10^{13} cm^{-2} over the 2-in. wafer. TEM cross section measurements of this AlGaN/GaN HEMT structure reveal large grains in the insulating, underlying GaN. Initial devices fabricated on the HEMT structure show no significant trapping effects. In agreement with the models of electrical conduction in polycrystalline semiconductors, increasing the GaN grain size has a large impact on improving electronic properties [17], especially the electron mobility.

Growth Pressure Influence on GaN Electronic Properties

Typically, to achieve the desired insulating GaN for HEMTs, growth pressures of 76 torr or less are used. If the insulating GaN has a high mobility when it is Si doped or a AlGaN layer is grown, the films are deemed suitable for HEMT devices. Recently, we have observed that the GaN films change from insulating at 49 torr to conductive (*n*-type) when the growth pressure is increased above 100 torr. The electron mobility reached a maximum at 250 torr where mobilities of 600 $cm^2V^{-1}s^{-1}$ with 9×10^{16} cm^{-3} *n*-type carriers were measured. We have tentatively assumed that the loss of the insulating GaN quality is due to a reduced

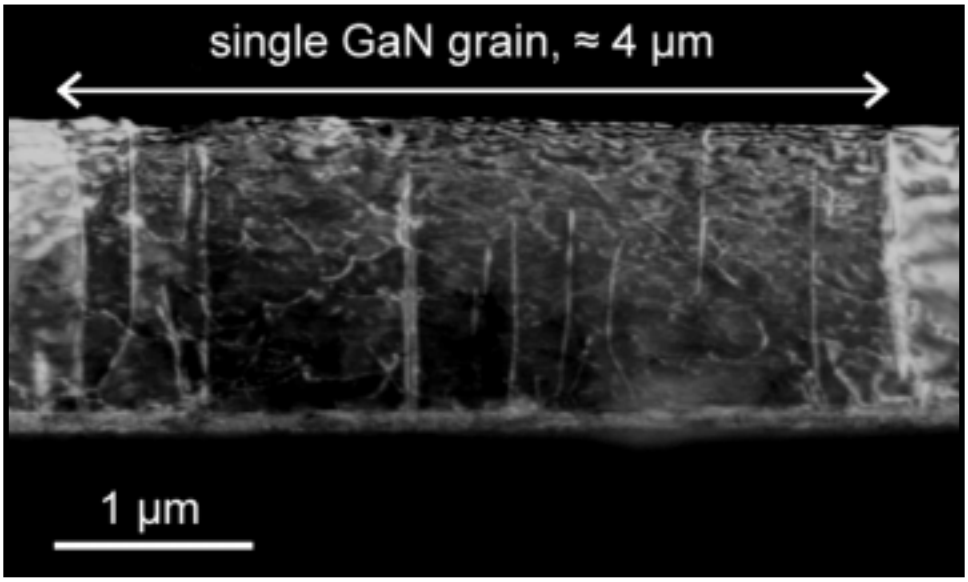

Fig. 9 - Shown is a TEM cross section of optimized GaN growth on sapphire. Individual GaN grains can be imaged by slightly tilting the GaN sample in the TEM.

deep acceptor (or trap) concentration. We are currently investigating the influence of growth pressure on GaN film quality and possible trapping-type defects, which are introduced at lower growth pressures.

Toward Identification of Trapping-Type Defects

Research is also underway at NRL to identify trapping-type defects. These defects have been observed to influence maximum operational frequency, power output, leakage current, current collapse, and transconductance dispersion [6]. Persistent photoconductivity (PPC) studies in a number of GaN device structures suggest a distribution of trap levels in the GaN material [18]. Previous device [6] and PPC [18] studies suggest that the traps are located in the insulating GaN.

At NRL, a spectroscopic method has been developed to detect and measure trapping-type influences in GaN FET device structures. Binari et al. previously observed that the drain current was restored in GaN MESFETs when light was applied [6]. Shorter wavelength light was found to be more efficient in restoring the drain current (i.e., decreasing the current collapse), suggesting the emission of trapped electrons through a photoionization process. The increase in the drain current in light vs dark (ΔI) normalized to the drain current in the dark (I_D) and the incident photon flux ($\Phi(h\nu)$) is plotted in Fig. 10(a) as a function of photon energy for GaN MESFET devices fabricated at NRL [19]. Two distinct trap levels are obtained from the fits. The photoionization spectrum is energy broadened because of strong coupling between the trap levels and the GaN vibrational levels as shown in Fig. 10(b). This vibronic coupling explains why a distribution of trap levels was initially proposed in the PPC studies. Further investigations of trapping-type defects are currently underway using photoluminescence, magnetic resonance, and current collapse spectroscopy (described above), which is unique because it directly measures the trap characteristics in working device structures.

Vertical Power Device Structures

If the assertion that grain size limits electron mobility in GaN films is true, device designs where the electrons do not cross grain boundaries should be considered. Electrons conducted vertically through the GaN will not scatter from grain boundaries. We are currently designing a vertical power transistor to test the benefits of this type of structure.

Future Research Focus

In this article, we have highlighted the current efforts in GaN materials growth, characterization, and device fabrication. Our research on GaN growth kinetics [11], GaN decomposition [12], and surface nitridation and nucleation layer growth [15] has been essential to achieving the high quality, high mobility GaN films described earlier. Our observation from TEM data that GaN grain size correlates with electron mobility [17] drove our selection of which growth parameters to vary. These insights allowed us to optimize GaN film growth in a new reactor design and achieve record mobilities for this reactor.

Although many GaN-based devices with outstanding properties have been fabricated, the scientific understanding necessary to routinely reproduce these results and advance device performance is currently lacking in many critical areas. This is especially true for many of the individual MOVPE growth steps that influence grain orientation and grain size. Further reduction in trap density is a high priority at NRL because such reduction should directly lead to improvements in device performance. This research is critical in order for GaN to reach its full potential for microwave power electronics.

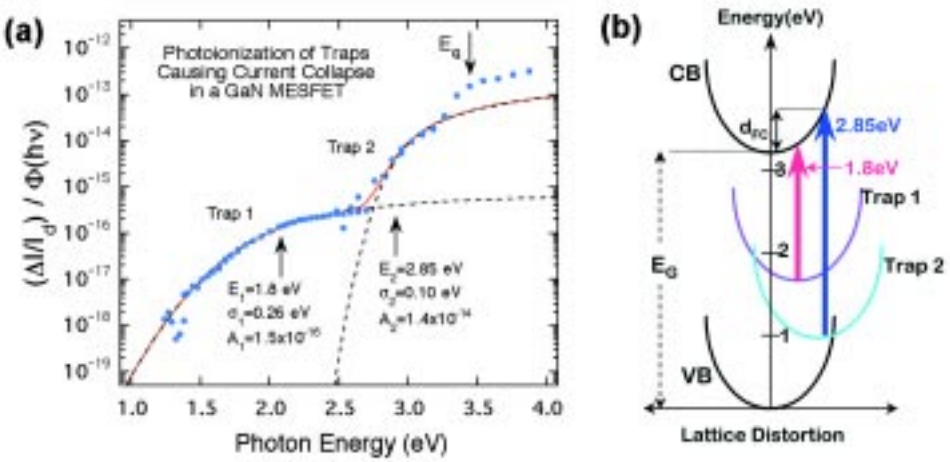

Fig. 10 - (a) The difference in drain current in light vs dark (ΔI) is plotted vs the photon energy. The value of ΔI is normalized to the drain current in the dark and to the photon energy. (b) The trap energy levels are plotted as a function of the lattice distortion. Vertical transitions between the trap energy levels and the conduction band (CB) lead to vibrational excitation of the lattice, which gives the appearance of a broadened distribution of trap energy levels.

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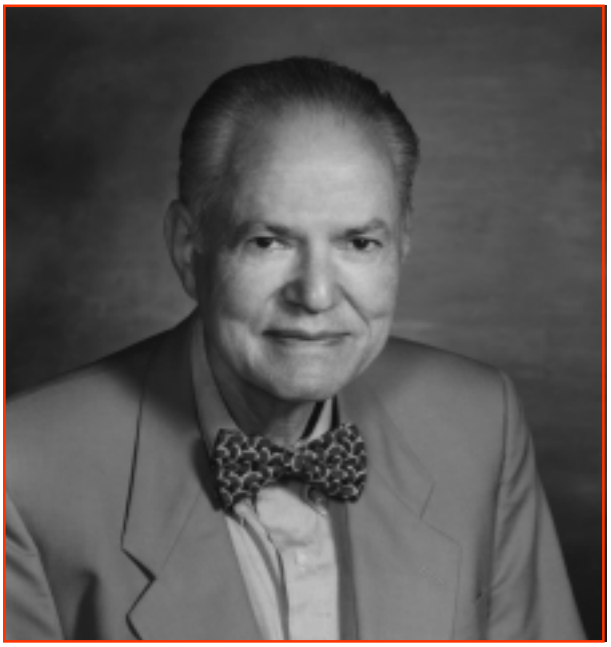
Mohammad Fatemi received his M.Sc. degree in theoretical physics in 1965 and his Ph.D. degree in physics in 1970 from the George Washington University. Since 1970, he has been active at NRL in the X-ray and neutron diffraction and topographic studies of strain-related phenomena in structural and electronic materials.

Profiles in Science



Dr. W.J. Choyke
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After receiving his Ph.D. in 1952 from Ohio State University, Jim Choyke joined Westinghouse Research Laboratories in Pittsburgh, Pennsylvania. He became an Adjunct Professor in the Physics Department of the University of Pittsburgh in 1974, and in 1988, after early retirement from Westinghouse, became a Research Professor of Physics. Currently, with his colleague Prof. Robert Devaty, he runs the Large Bandgap Laboratory of the Department.

In 1955 he met Lyle Patrick who had just come from the University of Chicago, and this led to a scientific collaboration on SiC that only ended with Patrick's early retirement in the mid-1970s. The first objective of this collaboration was to verify that all the common polytypes of SiC were indirect semiconductors. Indeed, this work went on concurrently with the famous study on the indirect transitions of Si at the Royal Radar Establishment in Malvern, England.

The next effort was stimulated by the theoretical work of Murray Lampert, then at Berkeley, on possible four-particle and three-particle exciton complexes in solids. Choyke and Patrick used low temperature photoluminescence to yield wonderfully sharp spectral lines for SiC, which led to a much better understanding of shallow impurity centers in SiC polytypes. The

researchers also noticed a forest of sharp lines at energies somewhat lower than the lines of the shallow centers. John Hopfield at Bell Labs explained such lines in GaP as donor-acceptor pairs. Many pair spectra were found in different polytypes of SiC, and the nitrogen-aluminum pair spectrum in cubic SiC (3C-SiC) led to a detailed analysis that yielded the ionization energy of the aluminum acceptor.

In collaboration with Don Feldman and Jim Parker at Westinghouse, Choyke began an extensive study of the vibrational properties of SiC polytypes using Raman scattering spectroscopy. They realized that the large unit cells of SiC, rather than being a complicating nuisance, could be exploited with "zone folding" to yield data in first-order Raman scattering, which is inaccessible in simple lattices such as Si. Zone folding is now commonly used in the study of quantum wells and superlattices. In the late 1960s, Choyke initiated studies to try to understand ion implantation in SiC. Since that time, many ion-induced defect centers have been unearthed. Annealing has also been studied to help bring this process under control for device fabrication. These studies also led to the discovery of hydrogen and deuterium centers in SiC well before they were recognized in the common semiconductors.

In the late 1970s, Choyke first studied electron-hole drops in a collaboration with the late Paul Dean of the Royal Signals and Radar Establishment in Malvern, England and Dieter Bimberg, currently a professor at the Technical University of Berlin, Germany. The mid-1980s brought new techniques for epitaxial growth of SiC, as well as the growth of boules of SiC, making large substrate wafers possible. Much purer and more controlled SiC now became available. In a close collaboration with several growth groups, an intense effort was started to study the conditions under which shallow and deep impurity states as well as defect states occur during growth. Today, better and better SiC and good band calculations have stimulated a number of current studies verifying theoretical predictions and unraveling age-old puzzles in SiC.

Professor Choyke has published approximately 320 scientific publications in major journals. He has also helped to edit several books, the latest of which is the two-volume *Silicon Carbide — A Review of Fundamental Questions and Applications to Current Device Technology* (1997), a combined effort with H. Matsunami in Kyoto and G. Pensl in Erlangen. Determined to keep promoting the growth of large bandgap semiconductors both scientifically and industrially as long as he can, Prof. Choyke continues to collaborate with colleagues in Europe and Japan and serves as co-program chairman with David Larkin of NASA's Glenn Space Center in Cleveland on ICSCRM'99.

Professor Choyke is a fellow of the AAAS and the American Physical Society. He was awarded the Westinghouse Award of Merit in 1983 and received the Alexander von Humboldt Research Prize in 1990. From 1993 to 1995, Prof. Choyke was chairman of the NRC Committee on Materials for High-Temperature Semiconductor Devices; this effort yielded a publication of the same name (National Academy Press, NMBA-474, Washington, D.C., 1995).

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